UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. FI996085

Total Pages in this Submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS

Box Patent Application Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES

and	invented	bv:

1) Roy Childs Flaker (deceased), 2) Louis L. Hsu, 3) Jente B. Kuang

If a CONTINUAT	ION APPLICA	TION, check appropriate box and supply the requisite information:
☐ Continuation	□ Divisional	☐ Continuation-in-part (CIP) of prior application no. 09/063,823
Which is a:		
☐ Continuation	\square Divisional	☐ Continuation-in-part (CIP) of prior application no
Which is a:		
☐ Continuation	☐ Divisional	☐ Continuation-in-part (CIP) of prior application no.

Enclosed are:

Application Elements

- 1.

 Filing fee as calculated and transmitted as described below
- 2. \(\Sigma \) Specification having \(\frac{20}{20} \) pages and including the following:
 - a.

 Descriptive Title of the Invention
 - b. 🗵 Cross References to Related Applications (if applicable)
 - c. ☐ Statement Regarding Federally-sponsored Research/Development (if applicable)
 - d.

 Reference to Microfiche Appendix (if applicable)
 - e.

 Background of the Invention
 - f.

 Brief Summary of the Invention

 - h. X Detailed Description
 - i. X Claim(s) as Classified Below
 - j.

 Abstract of the Disclosure

Application Elements (Continued)

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. FI996085

Total Pages in this Submission

3

3. Drawing(s) (when necessary as prescribed by 35 USC 113) 6 sheets
3. Ear Drawing(s) (which necessary as prescribed by 33 OSC 113) o sneets
a. 🗵 Formal Number of Sheets: 6
b. Informal Number of Sheets:
4. ⊠ Oath or Declaration
a. □ Newly executed (original or copy) □ Unexecuted
b. ⊠ Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional application only)
c. ☑ With Power of Attorney ☐ Without Power of Attorney
d. □ <u>DELETION OF INVENTOR(S)</u>
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference (usable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is
supplied under Box 4b, is considered as being part of the disclosure of the accompanying
application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche (Appendix)
7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all must be included)
a. □ Paper Copy
b. Computer Readable Copy (identical to computer copy)
c. □ Statement Verifying identical Paper and computer Readable Copy
Accompanying Application Parts
8. ☐ Assignment Papers (cover sheet and document(s))
9. □ 37 CFR 3.73(B) Statement (when there is an assignee)
10. ☐ English Translation Document (if applicable)
11. ☐ 37 CFR 3.73(B) Statement (when there is an assignee)
12. ☑ Preliminary Amendment
13. ☑ Acknowledgement postcard
14. Certificate of Mailing ☐ First Class ☐ Express Mail (Specify Label No.):

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. FI996085

Total Pages in this Submission

		Accompanying Applica	ation Parts (Continued)		
15. Certified C	Copy of Priority Doc	cument(s) (if foreign p	priority is claimed)		
16. □ Additional	Enclosures (please i	identify below):			
Information Di	isclosure Statement,	Forms PTO-1449 &	PTO-892		
<u> </u>		Fee Calculation	and Transmittal		
		CLĄIMS	AS:FILED	Las de la las de las de las de la las de la las de la las de	
For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	8	- 20 =	9	x \$18.00	\$0.00
Indep Claims	1	- 3 =	0	x \$0.00	\$0.00
Multiple Dependent	Claims (check if ap	plicable) 🏻			\$0.00
				BASIC FEE	\$690.00
OTHER FEE (speci	fy purpose)				\$0.00
			T	OTAL FILING FEE	\$690.00
No. 09-0458 as ☐ Charge the ☐ Credit any ☐ Charge any ☐ Charge the pursuant to	amount of \$690.00 overpayment. additional filing fee issue fee set in 37 C.F.R. 1.311(b)	es required under 37 (F.R. 1.18 at the mai	dit IBM Corporation is sheet is enclosed. C.F.R. 1.16 and 1.1	7.	
Date: 6-7-	-	Eric J. Franklin, Reg. I	No. 37,134 (Signatu	(L)	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

ROY CHILDS FLAKER (deceased) : Attorney Docket: F1996085

Serial No.: Con't of 09/063,823 : Art Unit: to be assigned

Filed: herewith : Examiner: to be assigned

For: CIRCUITS AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents Washington, DC 20231

Sir:

Prior to examination, please amend the above-identified application as follows:

In the Specification:

Page 1, line 1, after the title, please insert:

--This application is a continuation of U.S. patent application serial number 09/063,823, filed April 22, 1998, which claims priority from U.S. provisional patent application serial number 60/044,251 filed on April 23, 1997.--.

In the Claims:

Please cancel claims 1-5 without prejudice to their reentry.

Remarks:

Claims 6-13 are now pending in this case. Applicants have canceled claims 1-5, which were prosecuted in the parent application.

In the event that the Examiner believes that an interview would serve to facilitate the prosecution of this application, Applicants respectfully urge the Examiner to contact the undersigned at the telephone number listed below.

The undersigned hereby authorizes the Commissioner to charge any insufficient fees or credit any overpayment associated with this communication to deposit account no. 22-0185.

Respectfully submitted,

Date: 6-7-00

Eric J. Franklin, Reg. No. 37,134

Attorney for Applicants

Pollock, Vande Sande & Amernick

1990 M Street, N.W.

Washington, DC 20036-3425 Telephone: 202-331-7111 Facsimile: 202-293-6229

CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES

BACKGROUND OF THE INVENTION

1. Technical Field

This invention generally relates to integrated circuits. More specifically, the present invention relates to enhancing the performance of Silicon On Insulator (SOI) devices.

2. Background Art

for everyday activity. Integrated circuits are the components that give life to our electronic devices. Integrated circuits are found in widespread use throughout our country, in appliances, in televisions and personal computers, and even in automobiles. Additionally, manufacturing and production facilities are becoming increasingly dependant on the use of integrated circuits for operational and production efficiencies. Indeed, in many ways, our everyday life could not function as it does without integrated circuits. These integrated circuits are manufactured in huge quantities in our country and abroad. Improved integrated circuit manufacturing processes have led to drastic price reductions for these devices.

20 The traditional integrated circuits fabrication process is a series of steps by which a geometric pattern or set of geometric patterns is transformed into an

10

15

20

operating integrated circuit. An integrated circuit consists of superimposed layers of conducting, insulating, and transistor-forming materials. By arranging predetermined geometric shapes in each of these layers, an integrated circuit that performs the desired function may be constructed. The overall fabrication process typically consists of the patterning of a particular sequence of successive layers using various chemicals as etchants. Many different processes exist for creating a pattern on the silicon wafer, with different processes being specifically adapted to produce the desired type of integrated circuit.

One relatively new process for fabricating integrated circuit devices is commonly known as Silicon On Insulator (SOI). SOI devices are semiconductor devices which are formed within a thin silicon layer that overlies an electrically insulating region formed over an integrated circuit substrate material. This insulating region may include, for example, a layer of SiO₂ deposited over a semiconductor substrate material such as silicon or gallium arsenide. This fabrication process allows devices to be created which are electrically isolated from the substrate. SOI devices offer several advantages over conventional semiconductor devices.

For example, SOI devices typically have lower parasitic capacitances which, in turn, translate into faster switching times for the resulting circuits. In addition, the well-known but undesirable phenomenon of "latchup," which is often exhibited by conventional Complementary Metal-Oxide Semiconductor (CMOS) devices, is avoided when CMOS devices are manufactured using SOI fabrication processes. SOI devices are also less susceptible to the adverse effects of ionizing radiation and, therefore, tend to be more reliable in

10

15

20

25

applications where ionizing radiation may shorten the life of traditional integrated circuits.

The advantageous characteristics of SOI devices result from the dielectric isolation described above. While providing many advantages, this dielectric isolation also produces some difficulties not encountered with more conventional integrated circuit devices. In conventional devices, electrical interactions occur between the device substrate and the device active region, e.g. the currentcarrying portion of the device, such as the current channel of a Metal-Oxide Semiconductor Field Effect Transistor (MOSFET). Occasionally, accumulated charge in the device active region can alter the device threshold voltage V_{τ} (i.e., the voltage at which the current channel of an enhancement-mode MOSFET begins to conduct current). However, in conventional devices, this accumulated charge is readily removed through the substrate by applying an appropriate voltage to the substrate which attracts the accumulated charge away from the active layer, into the substrate, and out through a conductive lead. For example, a negative voltage applied to the substrate attracts holes from the active layer into the substrate, while a positive voltage attracts electrons. Alternatively, it is possible to change the threshold voltage of a conventional integrated circuit device, if desired, by applying a voltage to the active region through the electrically connected substrate. This is known as the "body effect."

In contrast, in a typical SOI device, the insulating region prevents both the conduction of charge from the active region into the substrate, and the application of a voltage to the active region through the substrate. Thus, the lack of flexibility in the operation of an integrated circuit device due to the SOI insulating region is often inconvenient. For example, during operation of a

10

15

20

25

typical SOI MOSFET, electrical charge can accumulate in the body of the device, (the region of the MOSFET between the source and the drain), until the concomitant electrical potential increases sufficiently to produce a shift in the threshold voltage (V_T) of the device. This shift can adversely affect the operation of the circuit and introduce errors into the information being processed by the device. The charge accumulates on the body of the SOI transistors in a circuit whenever the circuit is not being supplied with voltage.

For example, in a typical circuit using bulk CMOS devices, the body of an n-FET device will be connected to ground and the body of a p-FET device will be connected to the supply voltage (V_{DD}) . Therefore, even when no voltage is applied to the n-FET or the p-FET, the body potential is controlled by the connection to either ground or V_{DD} and the operational V_{T} will be in keeping with standard design parameters for each device. In contrast, the body of an SOI device is not connected to either ground or V_{DD} and, therefore, the body of the device can "float" to any voltage level. In addition, thermal fluctuations can also cause electrical charges to accumulate in the body of the transistors. Over a period of time, this charge can accumulate and can cause V_{T} to be lower than the specified design parameters and the transistor will switch on before it should. If V_{T} has been altered significantly, the operation of the circuit can be effected. For example, in synchronization circuits with critical timing requirements, the transistor may not switch on at the appropriate time and the circuit may not operate at all.

One specific example of the problems associated with SOI integrated devices is illustrated in FIG. 4. In FIG. 4, a typical memory circuit 400 with 256 local word line drivers comprises a highest order local word line

10

15

20

(LWL255) circuit 430 which includes transistor 432 and node 431; a lowest order local word line circuit (LWL0) 440; a segment driver 450 which includes a pass transistor 451; and a select line 460. The illustrated circuit represents a small portion (one segment) of a much larger memory array on a typical memory chip. The lowest order local word line (LWL0) circuit 440 is driven by a low order Global Word Line (GLW0). The highest order local word line (LWL255) circuit 430 is, correspondingly, driven by a high order Global Word Line 255 (GWL255). The intervening word lines (not shown) are likewise driven by other global word lines (not shown).

The individual segments in a memory array are accessed by activating segment driver 450. When memory circuit 400 is not being accessed, all of the global word lines are deselected and are at a low voltage level and, due to the operation of the transistors connected to GWL255 shown in circuit 430, node 431 is connected to V_{DD}. All of the remaining word lines circuits (GWL0-GWL254) operate in the same way. When segment driver 450 is not selected, transistor 432, and the corresponding transistors in the other local word driver circuits, are not driven and are therefore turned off. Circuit 435 represents the load of the remaining word line drivers. Due to the accumulated charge stored on each of the transistors represented by this load, select line 460 appears to circuit 400 as if it were a large capacitor with a stored charge.

When segment driver 450 is activated, one of the active global word lines will provide access to a local word line for reading or writing to a specific memory location. This process is accomplished as follows. The memory chip is activated by supplying a signal to the CLOCK input of segment driver 450.

25 The control (CTL) or segment signal is used to select one of the memory

15

20

subarrays or segments for reading or writing. After a small propagation delay, the control circuit (not shown) creates a decoding signal DECODE that activates the appropriate subarray by driving select line 460 to low. When all three of the input signals to segment driver 450 are active, node 431 in the local word line driver circuit 430 is discharged through select line 460 and pull-down transistor 451 in segment driver 450.

At this point, although only one of the 256 global word lines is selected, segment driver 450 must discharge all of the accumulated charge in the body of each transistor corresponding to transistor 432 in local word line driver 430 for each of the 256 local word line drivers. This is known as "fan-out" loading. As described earlier, the bodies of the SOI transistors have a tendency to accumulate electrical charge. When a given memory segment is not being accessed for a period of time (i.e. 0.1ms for a typical n-FET device), an electrical charge can accumulate in the body of each one of the SOI transistors. Then, when the memory segment is first accessed, the charge on each of the transistors corresponding to transistor 432 must be discharged. The "first access" is considered to be when the segment is first used to read or write data after a period of inactivity. If subsequent accesses are to the same memory segment, no charge sufficient to cause delays will have been accumulated. If. however, a different memory segment is subsequently accessed, the previously accessed memory segment may, once again, need to be discharged prior to subsequent accesses. Memory access is delayed until the electrical charge is dissipated.

The fan-out loading effect is known for a tendency to slow down memory access times associated with SOI devices, especially during the first cycle of

10

15

20

25

operation, when the accumulated charge on the body of the transistors is the greatest. Also, the greater the physical distance between segment driver 450 and the selected local word line driver, the harder it is to drive. Due to the propagation delay inherent in the physical circuit wiring, body charges in more distant devices take longer to discharge through the long, relatively resistive wire. However, after the first access cycle, the SOI loading effect is diminished significantly. This is because, once the accumulated body charges in all of the N-channel FET pull-down devices have been discharged, a relatively long period of time is needed to build up the charge on the body of the transistors again. Therefore, as long as the memory access requests are to the same subarray or segment, there will be no additional access delay associated with discharge propagation delays. By logical extension, the worst access times for an SOI memory device is generally the first access cycle for a device that is located the farthest distance from segment driver 450.

The loading effect described above can be completely eliminated by connecting the body of an SOI device to a reference ground. Referring now to FIG. 7, a SOI transistor 700 formed with a body contact for connecting the body of transistor 700 to ground is shown. SOI transistor 700 has a body implant mask region 710, a source/drain implant mask region 720, a T-shaped gate 725; a source contact 730, a drain contact 740, and a body contact 750. Body contact 750 is typically connected to ground for an n-channel device and to V_{DD} for a p-channel device. The creation of body contact 750 requires additional processing and mask steps when transistor 700 is being fabricated. If body contact 750 is connected to ground, the problems associated with charge build-up on the body of transistor 700 are eliminated. However, this will also negatively impact circuit operation in at least two ways. First, circuit overhead (i.e. the amount of

10

15

area needed to fabricate the circuit) is significantly increased and, second, the speed advantage inherent in SOI circuits is also eliminated, because the lower variable V_T of SOI devices is not longer present.

Therefore, there exists a need to provide a way to take advantage of the benefits of SOI device characteristics without suffering the possible negative implications of SOI fabricated devices. In addition, the methods employed should not unnecessarily diminish or destroy the positive advantages provided by implementing circuits and devices using SOI technology.

DISCLOSURE OF INVENTION

According to the present invention, a circuit and methods for enhancing the operation of SOI fabricated devices are disclosed. In a preferred embodiment of the present invention, a pulse discharge circuit is provided. Here, a circuit is designed to do a pulse discharge that will eliminate the accumulated electrical charge on the SOI devices in the memory subarray just prior to the first access cycle. As explained above, once the accumulated charge has been dissipated, the speed penalty for successive accesses to the memory subarray is eliminated or greatly reduced. With a proper control signal, timing and sizing, this can be a very effective method to solve the problem associated with the SOI loading effect.

Alternatively, instead of connecting the bodies of all SOI devices in a memory circuit to ground, the bodies of the speed-critical devices are selectively connected to a reference ground. This would enable the circuit to retain most of the speed advantages associated with SOI devices while overcoming the loading

problem described above. With this preferred embodiment of the present invention, the major delay caused by the bipolar loading effect is minimized while the speed advantage due to providing a low Vt effect is preserved. The overall body resistance of the individual devices has a minimal effect on the device body potential.

The foregoing and other features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

- The preferred embodiments of the present invention will hereinafter be described in conjunction with the appended drawings, where like designations denote like elements, and:
 - FIG. 1 is a perspective view of a portion of a bulk CMOS wafer:
 - FIG. 2 is a perspective view of a portion of an SOI wafer;
- FIG. 3 is a block diagram of a circuit according to a preferred embodiment of the present invention;
 - FIG. 4 is a schematic of a local word line driver array for a typical memory circuit;
- FIG. 5 is a block diagram of the circuit of FIG. 4 including a dynamic pulse discharge circuit according to a preferred embodiment of the present invention;

FIG. 6 is a schematic of the circuit of FIG. 5 including a dynamic pulse discharge circuit according to a preferred embodiment of the present invention; and

FIG. 7 is a plan view of an SOI transistor fabricated with a body contact.

BEST MODE FOR CARRYING OUT THE INVENTION

The present invention relates to the use and operation of integrated circuit transistors, particularly SOI transistors. For those individuals who are not familiar with CMOS and SOI fabricated devices, the Overview section below presents some basic concepts that will help to understand the invention. Those who are skilled in the art may wish to skip this section and begin with the Detailed Description Section instead.

<u>OVERVIEW</u>

5

10

15

20

Referring now to FIG. 1, a portion of a typical bulk CMOS wafer 100 includes: a substrate 110; an n-well 120; an n-well contact 125; a p-well 130; n⁺ source and drain diffusions 135; polysilicon gate contacts 140; p⁻ source and drain diffusions 145; a p-well contact 155; a surface isolation 160; an n-channel 170; an n-body 175; a p-channel 180; a p-body 185, and a gate oxide 190.

The designation of a particular device as a p-channel device or an n-channel device depends on the type of fabrication process used to create the device. Substrate 110 is any semiconductor material known to those skilled in the art. The various wells and contacts are created by using different types of constituents when the wafer is being fabricated. In normal operation, n-well contact 125 is connected to V_{DD} and p-well contact 155 is connected to ground.

15

20

25

Referring now to FIG. 2, a portion of a typical SOI wafer 200 includes: a substrate 210; polysilicon gate contacts 140; a buried oxide layer 220; and an active region 230. Active region 230 is a thin layer of silicon and includes n source and drain diffusions 135; p source and drain diffusions 145; a surface isolation 160; an n-channel 170; a n-body 175; a p-channel 180; a p-body 185, and gate oxide 190.

Substrate 210 is any semiconductor material, or metal, or glass, known to those skilled in the art. Source and drain diffusions 135 and 145 will typically abut buried oxide layer 220. Surface isolation 160 and buried oxide layer 220 serve to electrically isolate source and drain diffusions 135 and 145, preventing electrical charge from being transferred to and from the devices through substrate 210.

DETAILED DESCRIPTION

Referring now to FIG. 3, a circuit 300 in accordance with a preferred embodiment of the present invention comprises: a pulse body discharge circuit 310; a circuit A 320; a circuit B 330; a control signal 340; an operation signal 350; a transistor 360; a reference ground 370; and a discharge path 380. Circuit 320 and circuit 330 may be any type of analog or digital logic device or circuit, including nand gates, memory circuits, microprocessors, and microcontroller circuits. Other examples of circuits 320 and 330 include voltage regulators, clock generation circuits, etc. In operation, transistor 360 acts as a switch for interconnecting circuits 320 and 330 whenever operation signal 350 is activated. Operation signal 350 is generated by a control circuit (not shown). Pulse body discharge circuit 310 can be used to enhance the switching speed of transistor 360. Just prior to activating operation signal 350, control signal 340 is

10

15

20

25

activated. Control signal 340 is also activated by the control circuit. When control signal 340 is activated, pulse body discharge circuit 310 provides a path from transistor 360 to reference ground 370 via discharge path 380. Therefore, before transistor 360 is activated by operation signal 350, the body of transistor 360 is completely discharged.

Referring now to FIG. 5, a memory circuit 500 in accordance with a preferred embodiment of the present invention includes: a pulse generator 510 that is a part of a dynamic pulse discharge circuit 310; local word line drivers 430 and 440; a segment driver 450; a select line 460; and the various signals explained in conjunction with FIG. 4 above. This figure illustrates how the circuit of FIG. 3 can be adapted for use in a computer memory application to provide faster switching times for memory circuit 500. Pulse generator 510 provides the discharge pulse that discharges the bodies of the SOI devices in memory circuit 500. Dynamic pulse discharge circuit 310 and pulse generator 510 are described in greater detail below.

Referring now to FIG. 6, memory circuit 500 of FIG. 5 is shown in schematic form. The components shown in memory circuit 500 are the same as in FIG. 5. Memory circuit 500 with 256 local word line drivers includes: a highest order local word line (LWL255) circuit 430; a lowest order local word line circuit 440; a segment driver 450; and a select line 460. As before, memory circuit 500 represents a small portion (one segment) of a much larger memory array on a typical memory chip. Lowest order local word line (LWL0) circuit 440 is driven by a low order Global Word Line (GLW0). Highest order local word line (LWL255) circuit 430 is, correspondingly, driven by a high order Global Word Line 255 (GWL255). The intervening word lines (not shown) are likewise driven by other global word lines (not shown). The

10

15

20

25

individual segments in a memory array are accessed by activating segment driver 450.

When segment driver 450 is activated, the active global word line will provide access to a local word line for reading or writing to a specific memory location. This process is accomplished as follows. The memory chip is activated by supplying a signal to the CLOCK input of segment driver 450. The control (CTL) or segment signal is used to select one of the memory subarrays or segments for reading or writing. In circuit 500, CTL is also supplied as an input signal to pulse discharge circuit 310. After a small propagation delay, the control circuit (not shown) creates a decoding signal DECODE that activates the appropriate subarray by connecting select line 460 to ground. When all three of the input signals to segment driver 450 are active, select line 460 is used to discharge the accumulated charge on the SOI transistors. This time, instead of discharging through segment driver 450 as shown in FIG. 4, the accumulated charge is dissipated through a pull-down transistor in inverter 624 which is located in pulse discharge circuit 310. This is accomplished as follows. In normal operation, to select a given memory subarray, the CTL signal for that subarray transitions from low to high. This CTL signal is also supplied to pulse discharge circuit 310 as an input signal. After a brief propagation delay through a delay element (invertors or other circuit device), circuit node 621 will transition from high to low. Circuit node 622 will generate a negative pulse and, after passing through an inverter, becomes a positive pulse at node 623. The positive signal or pulse applied to transistor 625 activates transistor 625 which, in turn, provides a path for discharging the word line drivers of memory circuit 500 through inverter 624. The pulse discharge signal generated by pulse generator 520 is the output signal from the pulse discharge circuit and, in a

10

preferred embodiment of the present invention, is supplied to the memory subarray just prior to the selection of the subarray for access. This means that the charge accumulated on the bodies of the SOI transistors has already been discharged when the request to access the subarray is received. By removing the charge before the first access occurs, the access time to the subarray is greatly enhanced. While it is possible to provide a discharge pulse prior to every access, this is not necessary. Once the initial accumulation of charge has been dissipated, as long as subsequent accesses are to the same subarray, there will not be very much charge accumulated in the subarray. By discharging the subarray prior to the first access only, the additional power requirements necessary to implement the invention are minimal. Once the control signal has selected a given segment, the control signal remains high and no transition of control signal is

Another preferred embodiment of the present invention utilizes selective 15 connection of the body of SOI devices to reference ground which, as discussed above in reference to FIG. 7, will require some additional space on a typical chip. To use this method, the specific devices in a given circuit which are most critical to circuit access and performance time are identified and the bodies of those devices are connected to ground or V_{DD}. All other SOI devices in the 20 circuit remain floating. For example, in FIG. 4, the body of transistor 432, and all other corresponding transistors in the other word line driver circuits, would be connected to ground. This method will successfully overcome most of the delays associated with the loading effect for circuit 400 during the first access cycle. However, because of the R/C delays described above, access to the top-25 most line driver in a memory circuit will still be much slower than for those line drivers located closest to the segment driver.

In summary, using a pulse body node discharge circuit can improve the access/switching time of SOI memory devices significantly. If the discharge pulse is only applied when first accessing a new subarray or segment, the extra power consumed will be negligible. In addition, the extra circuitry required to generate the pulse is negligible and can be added to a typical circuit layout without adversely impacting the overall chip size. If, on the other hand, the discharge pulse is applied to every memory access cycle, the access speed of the SOI memory device can be optimized. This implementation will cause some additional power consumption but remains desirable for those applications where high-speed memory access is necessary.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

CLAIMS

1	1.	In a circuit comprising a plurality of SOI devices wherein each of the
2		plurality of SOI devices has a body, a mechanism for enhancing the
3		performance of the circuit, the mechanism comprising:
4		a circuit component for discharging accumulated electrical potential from
5		the body of the plurality of SOI devices.
1	2.	The mechanism of claim 1 wherein the circuit component comprises a
2		pulse discharge circuit.
1	3.	The mechanism of claim 1 wherein the circuit component comprises a
2		connection to ground for at least one of the bodies of the SOI devices.
1	4.	The mechanism of claim 2 wherein the pulse discharge circuit comprises:
2		an input signal;
3		a delay element coupled to the input signal; and
4		an output signal coupled to the input signal, the output signal driving the
5		circuit

- 1 5. The mechanism of claim 2 wherein the pulse discharge circuit further comprises a pulse generator.
- 1 6. In a circuit comprising at least one SOI device, a method for enhancing the performance of the circuit, the method comprising the steps of:
- providing a pulse discharge circuit connected to the at least one SOI
- 4 device;
- 5 using the pulse discharge circuit to discharge any accumulated potential on
- 6 the at least one SOI device prior to accessing the at least one SOI device.
- 1 7. The method of claim 6 wherein the circuit comprises a memory circuit.
- 1 8. The method of claim 6 wherein the pulse discharge circuit compises:
- 2 an input signal;
- a delay element coupled to the input signal; and
- an output signal coupled to the input signal, the output signal driving the
- 5 circuit.

- 9. In a circuit comprising a plurality of SOI devices wherein each of the plurality of SOI devices has a body, a method for enhancing the performance of the circuit, the method comprising the step of:

 selecting grounding the body of at least one of the plurality of SOI devices to dissipate electric potential.
- 1 10. The circuit of claim 9 wherein the plurality of SOI devices comprises a memory circuit.

1	11.	In a circuit comprising a plurality of SOI devices wherein each of the
2		plurality of SOI devices has a body, a method for enhancing the
3		performance of the circuit, the method comprising the step of:
4		providing a pulse discharge circuit, the pulse discharge circuit having a
5		pulse generator and the pulse generator being connected to the circuit;
6		using the pulse generator to generate a pulse;
7		discharging any accumulated potential on the body of at least one of the
8		plurality of SOI devices by supplying the pulse from the pulse generator t
9		the body of the at least one of the plurality of the SOI devices at a pre-
10		determined time.
1	12.	The method of claim 11 wherein the plurality of SOI devices comprises a
2		memory circuit.
1	13.	The method of claim 12 wherein the pre-determined time is just prior to
2		accessing the memory circuit for reading or writing data.

10

15

20

ABSTRACT OF THE DISCLOSURE

CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES

According to the present invention, a circuit and methods for enhancing the operation of SOI fabricated devices are disclosed. In a preferred embodiment of the present invention, a pulse discharge circuit is provided. Here, a circuit is designed to provide a pulse that will discharge the accumulated electrical charge on the body of the SOI devices in the memory subarray just prior to the first access cycle. As explained above, once the accumulated charge has been dissipated, the speed penalty for successive accesses to the memory subarray is eliminated or greatly reduced. With a proper control signal, timing and sizing, this can be a very effective method to solve the problem associated with the SOI loading effect. Alternatively, instead of connecting the bodies of all SOI devices in a memory circuit to ground, the bodies of the N-channel FET pull-down devices of the local word line drivers can be selectively connected to a reference ground. This would enable the circuit to retain most of the speed advantages associated with SOI devices while overcoming the loading problem described above. With this preferred embodiment of the present invention, the major delay caused by the bipolar loading effect is minimized while the speed advantage due to providing a lower, variable Vt effect is preserved. The overall body resistance of the individual devices has a minimal effect on the device body potential.

1/6 HSU et ai SMM FI9-96-085

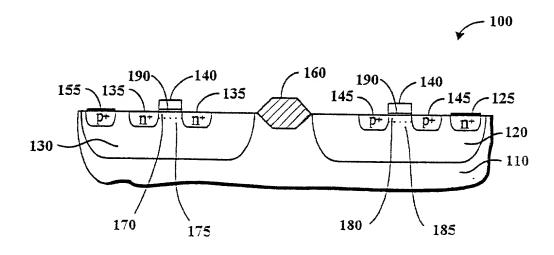


FIG. 1

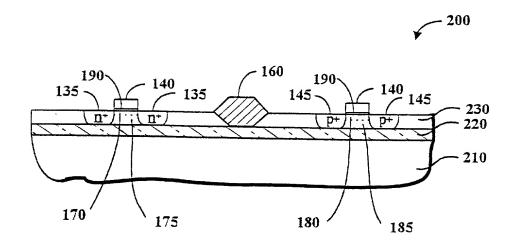


FIG. 2

2/6 FI9-96-085

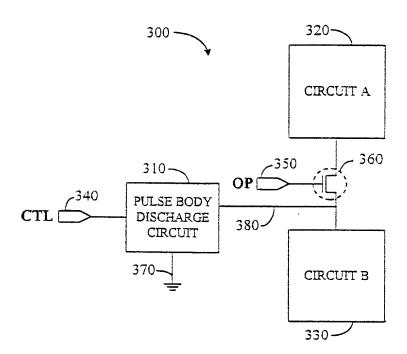


FIG. 3

3/6 FI9-96-085

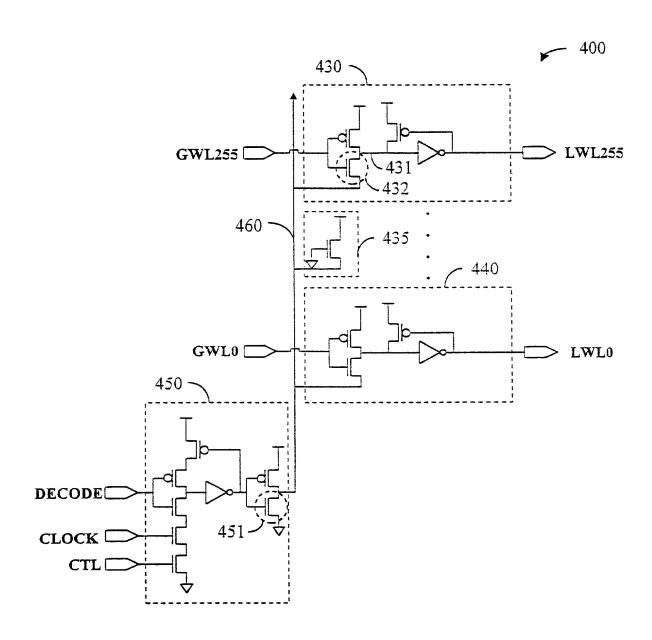
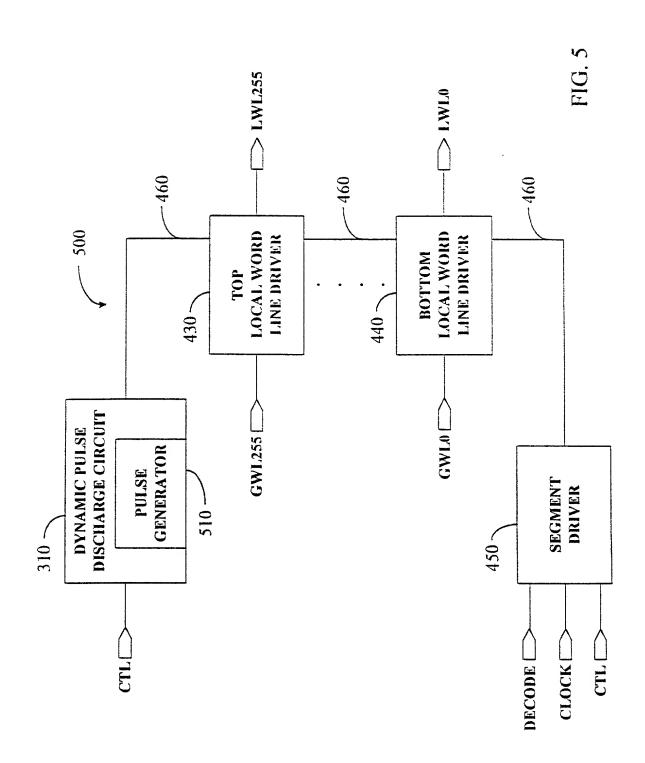
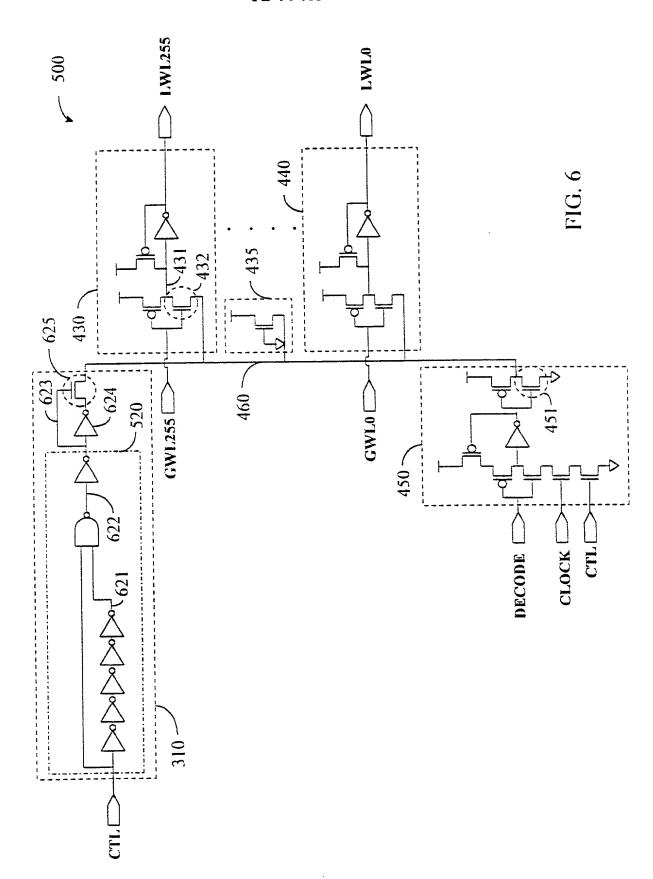


FIG. 4

4/6 FI9-96-085



5/6 FI9-96-085



6/6 FI9-96-085

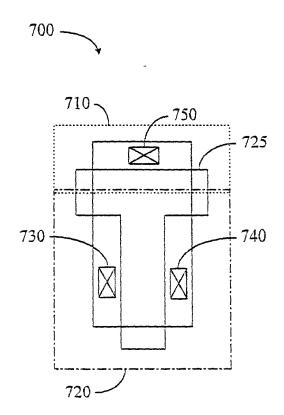


FIG. 7

DECLARA	ATION FOR P	ATENT APPI	LICATION		
As a below-named inventor, I h	ereby declare that:				
My residence, post office add I believe I am the original, firs of the subject matter which is clai	t and sole inventor (if of med and for which a p	only one name is listed patent is sought on the	helow) or an original first a		names are listed below)
the specification of which: (check	c one)				
[XX] is attached hereto.	was filed on	as United S and was amended	tates Patent Application Ser	ial No. or PCT Internations (if applicable).	al Application Number
I hereby state that I have review referred to above.	wed and understand the	contents of the above	-identified specification, inc	luding the claims, as amend	ied by any amendment
I acknowledge the duty to dis- Prior Foreign Application(s): inventor's certificate listed below. America, listed below and have also on which priority is claimed:	l hereby claim foreign or § 365(a) of any PC	priority benefits under CT international applic	35 U.S.C. § 119(a)-(d) or station which designated at	365(b) of any foreign applicant one country other than	ication(s) for patent or in the United States of that of the application Priority Claimed
(Application No.)		(Country)		Day/Month/Year Filed)	[] [] Yas No
(Application No)		(Country)	(I	Day/Month/Year Filea)	[] [] 7es No
(Application No.)		(Country)		Day/Month/Year Filed)	∵ l [] Yes No
I hereby claim the benefit unde of this application is not disclosed to disclose material information as international filing date of this app	in the prior United Stat defined in 37 CFR §	tes application in the m	nanner provided by 35 U.S.	C. 8 117 first naragraph I	acknowledge the dury
(U.S. Application Se	rial No.)	(U.S. Filing Da	te)	(Statuspatented, pending	z, abandoned)
(U.S. Application Se I hereby appoint the following atto therewith: Joseph P. Abate, Reg. No. 39,306; D. Mortinger, Reg. No. 32,440, Marc D. Soucar, Reg. No. 32,440, Marc D. No. 16,906, George Vande Sande, 24,351, Richard Wiener, Reg. No. George R. Pettit, Reg. No. 27,369, Wales, Reg. No. 39,413; all of POL A. Pennington, Reg. No. 32,588; J	rneys and/or agents to lo. 30.382; Aziz M. Al aryl K. Neff. Reg. No. Schechter, Reg. No. 28 Reg. No. 17.276, Robe 18.741, Townsend M. Louis Woo, Reg. No. LOCK, VANDE SAN	hsan, Reg. No. 32,100 38,253; Eric W. Petr 1,989; all of INTERNA ert R. Priddy, Reg. No. Belser, Jr., Reg. No. 31,730. Elzbieta Chic IDE & PRIDDY; John	tion and transact all busine to Ira D. Blecker, Reg. No. aske, Reg. No. 28,459, H. TIONAL BUSINESS MAC 20,169, Burton A. Amerni 22,956; Morris Liss, Reg. pecka, Reg. No. 32,767, E. E. Hoel, Reg. No. 26,279.	29.894: Steven Capeila, Re Daniel Schnurmann, Reg. CHINES CORPORATION: ick. Reg. No. 24.852, Stant No. 24.510, Martin Abramic J. Franklin, Reg. No. 37 Christopher A. Hughes Reg.	nark Office connected eg. No. 33.086: Alison No. 35.791, Steven J. Elliott I. Pollock, Reg. ey B. Green, Reg. No. son, Reg. No. 25.787.
Send Corres	spondence and Direct George Vande Sar (202) 331-7111	nde		eorge Vande Sande nde Sande & Priddy, R.L P.O. Box 19088	.L.P.
I hereby declare that all statementrue: and further that these statementor both, under 18 U.S.C. § 1001 as	its are made with the ki	nowledge that willful t	rue and that all statements takes statements and the like	nade on information and be so made are punishable by	elief are believed to be
Full name of sole or first inventor (heir)	or Roy Chi	lds Flaker	c (deceased)	by Catherin	ne O'Brien
Inventor's Signature	hein O	Min		Date X 4/6	9/08
Residence Address 2 Ridge	e Road, Ess	sex Junctio	on, Vermont 0		

[X] See next page for additional inventors

Citizenship <u>United States</u>

Post Office Address Same as Above

Page Two

Full name of second joint inventor (if any): Louis L. Hsu	
Inventor's Signature	Date
Residence Address 7 Crosby Court, Fishkill, New York 12524	
Citizenship <u>United States</u>	
Post Office Address Same as Above	
Inventor's Signature	
Residence Address 15 Four Winds Drive, Poughkeepsie, New York	Date
Citizenship Tarwan R.O.C.	12503
Post Office Address Same as Above	
Fuil name of fourth joint inventor (if any):	
Inventor's Signature	Date
Residence Address	
Citizenship	
Post Office Address	
Full name of fifth joint inventor (if any):	
Inventor's Signature	Date
Residence Address	
Citizenship	
Post Office Address	
Full name of sixth joint inventor (if any):	
Inventor's Signature	Date
Residence Address	
Citizenship	
Post Office Address	
Full name of seventh joint inventor (if any):	
Inventor's Signature	Date
Residence Address	
Citizenship	
Post Office Address	
Full name of eighth joint inventor (if any):	
	Date
Residence Address	
Citizenship	
Post Office Address	

As a below-named inventor. I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

the specific	cation of which:	(check o	ne)			
[XX] is a	nttached hereto.	11	was filed on		ntent Application Serial No. or PCT Internations 19 (if applicable).	al Application Number
I hereb		reviewe	d and understand t	he contents of the above-identif	ied specification, including the claims, as amend	ded by any amendment
Prior F inventor's America, li	oreign Application certificate listed b	n(s): Ih elow.on ve also i	ereby claim foreig r § 365(a) of any	n priority benefits under 35 U.S PCT international application of	lity of this application in accordance with 37 C S.C. § 119(a)-(d) or §365(b) of any foreign application designated at least one country other that or inventor's certificate having a filing date before	ication(s) for patent or in the United States of
		•				Priority Claimed
	Application No.)			(Country)	(Day/Month/Year Filed)	[][] Yes No
(1	Application No.)			(Country)	(Day/Month/Year Filed)	[] [] Yes No [] []
(,	Application No.)			(Country)	(Day/Month/Year Filed)	Yes No
I hereb	by claim the benef	it under	Application No.		nited States provisional application(s) listed belo	ow.
			60/044 251	'	April 23, 1997	
to disalasa	, .			tates approactors in the intainter	provided by 35 U.S.C. § 112, first paragraph, I	acknowledge the duty
	al tiling date of the	is applic	defined in 37 CFR cation:		provided by 35 U.S.C. § 112, first paragraph, I ween the filing date of the prior application ar (Status—patented, pendin	nd the national or PCT
I hereby at therewith: D. Morting Soucar, Re No. 16.906 24,351, Ri George R. Wales, Res	(U.S. Application (U.S. Applic	tion Seria tion Seria tion Seria tion Seria tion Seria tion O.6; Dara tion D. Sc sande. R g. No. 1 7.369. L Dof POLL	al No.) al No. al	(U.S. Filing Date) (U.S. Filing Date) (U.S. Filing Date) to prosecute this application at Ahsan, Reg. No. 32,100: Ira E No. 38,253; Eric W. Petraske, 28,989; all of INTERNATION obert R. Priddy, Reg. No. 20,16 M. Belser, Jr., Reg. No. 22,95 No. 31,730. Elzbieta Chlopecka ANDE & PRIDDY, John E. Ho	ween the filing date of the prior application ar	g, abandoned) g, abandoned) g, abandoned) mark Office connected eg. No. 33.086: Alison No. 35,791. Steven J. Elliott I. Pollock, Reg. ley B. Green, Reg. No. nson, Reg. No. 25.787. 7.134 and Robert Scott
I hereby at therewith: D. Morting Soucar, Re No. 16.906 24,351, Ri George R. Wales, Res A. Penning	(U.S. Applicat (U.S. Applicat	ion Seria ion Seria ion Seria ing attorn Reg. No 06; Dar irc D. Sc sande. R g. No. 1 7.369. L of POLL 588: Jos Corresp	defined in 37 CFR eation: al No.) al No.) al No.) teys and/or agents . 30.382; Aziz M. yi K. Neff, Reg. No. thechter, Reg. No. 28,741. Townsend .ouis Woo, Reg. N. OCK, VANDE Saseph C. Redmond. condence and Direct George Vande (202) 331-71 tes made herein of	(U.S. Filing Date) (U.S. Filing Date) (U.S. Filing Date) to prosecute this application at Ahsan. Reg. No. 32,100: Ira E No. 38,253; Eric W. Petraske. 28,989; all of INTERNATION. Obert R. Priddy. Reg. No. 20,16 M. Belser, Jr., Reg. No. 22,95 Io. 31,730. Elzbieta Chlopecka ANDE & PRIDDY, John E. Ho. Jr., Reg. No. 18,753, all of Met Telephone Calls to Sande	(Status-patented, pendin (Status-patented, pendin (Status-patented, pendin (Status-patented, pendin nd transact all business in the Patent and Trade D. Blecker, Reg. No. 29.894; Steven Capella, R. Reg. No. 28.459. H. Daniel Schnurmann, Reg. AL BUSINESS MACHINES CORPORATION: 69. Burton A. Amernick, Reg. No. 24.852. Stan 6: Morris Liss, Reg. No. 24.510. Martin Abran, Reg. No. 32.767, Eric J. Franklin, Reg. No. 3 el. Reg. No. 26.279. Christopher A. Hughes, Red (ORGAN & FINNEGAN, L.L.) George Vande Sande Pollock, Vande Sande & Priddy, R. P.O. Box 19088 Washington, D.C. 20036-3425 Und that all statements made on information and but the statements made on information and the st	g, abandoned) g, abandoned) g, abandoned) mark Office connected eg. No. 33.086: Alison No. 35,791. Steven J. Elliott I. Pollock. Reg. ley B. Green. Reg. No. 135,781. Steven J. 25,787. 7.134 and Robert Scott eg. No. 26,914. Edward L.L.P. L.L.P. L.S.A. belief are believed to be
I hereby at therewith: D. Morting Soucar, Re No. 16.906 24,351, Ri George R. Wales, Res A. Penning I hereb true: and fi	(U.S. Applicate of the (U.S. Applicate opening the following Joseph P. Abate, 19 ger. Reg. No. 39,3 g. No. 32,440, May George Vande Schard Wiener, Reg. No. 22 g. No. 39,413; all ogton. Reg. No. 32. Send	ion Seria ion Seria ion Seria ing attorn Reg. No 06; Dar irc D. So lande. R g. No. 1 7.369. L of POLL 588: Jos Corresp	defined in 37 CFR eation: al No.) al No.) al No.) teys and/or agents. 30.382: Aziz M. yi K. Neff, Reg. No. teechter, Reg. No. eg. No. 17.276. Re 8,741. Townsend ouis Woo, Reg. N. OCK, VANDE Se seph C. Redmond. ondence and Direct George Vande (202) 331-71 tts made herein of stare made with the	(U.S. Filing Date) (U.S. Filing Date) (U.S. Filing Date) to prosecute this application at Ahsan. Reg. No. 32,100: Ira E No. 38,253; Eric W. Petraske. 28,989; all of INTERNATION. Obert R. Priddy. Reg. No. 20,16 M. Belser. Jr., Reg. No. 22,95 Io. 31,730. Elzbieta Chlopecka ANDE & PRIDDY. John E. Ho. Jr., Reg. No. 18,753, all of M. ot Telephone Calls to Sande 111 my own knowledge are true are knowledge that willful false s	(Status-patented, pendin India transact all business in the Patent and Trade (O. Blecker, Reg. No. 29.894; Steven Capella, R Reg. No. 28,459. H. Daniel Schnurmann, Reg. AL BUSINESS MACHINES CORPORATION: 59. Burton A. Amernick, Reg. No. 24.852. Stan 6: Morris Liss, Reg. No. 24.510. Martin Abran 10. Reg. No. 32.767, Eric J. Franklin, Reg. No. 3 11. Reg. No. 26.279. Christopher A. Hughes, Ref 12. George Vande Sande 13. Polick, Vande Sande & Priddy, R.I 14. P.O. Box 19088 15. Washington, D.C. 20036–3425	ig, abandoned) ig, abandoned) ig, abandoned) mark Office connected eg. No. 33.086: Alison No. 35,791. Steven J. Elliott I. Pollock. Reg. ley B. Green. Reg. No. nson. Reg. No. 25.787. 7.134 and Robert Scott eg. No. 26.914. Edward L.L.P. L.L.P. celief are believed to be y tine or imprisonment.
I hereby at therewith: D. Morting Soucar, Re No. 16.906 24,351, Ri George R. Wales, Res A. Penning I hereb true: and fi or both. ur	(U.S. Applicat (U.S. Applicat (U.S. Applicat (U.S. Applicat point the followir Joseph P. Abate, It ger. Reg. No. 39,3 g. No. 32,440, Ma b. George Vande S chard Wiener, Reg. Pettit, Reg. No. 2 g. No. 39,413; all (gton, Reg. No. 32. Send sy declare that all surther that these stader 18 U.S.C. § 1 of sole or first inv	ion Seria ion Seria ion Seria ing attorn Reg. No 06; Dara irc D. So sande. R g. No. 1 7.369. L of POLL 588: Jos Corresp	defined in 37 CFR eation: al No.) al No.) al No.) teys and/or agents. 30.382: Aziz M. yi K. Neff, Reg. No. tees. No. 17.276. Re 8,741. Townsend. ouis Woo, Reg. N. OCK, VANDE Se seph C. Redmond. ondence and Direc George Vande. (202) 331-71 tes made herein of s are made with the d that such willful	(U.S. Filing Date) (U.S. Filing Date) (U.S. Filing Date) to prosecute this application at Ahsan. Reg. No. 32,100: Ira E No. 38,253; Eric W. Petraske. 28,989; all of iNTERNATION. Obert R. Priddy. Reg. No. 20,16 M. Belser. Jr., Reg. No. 22,95 Io. 31,730. Elzbieta Chlopecka ANDE & PRIDDY. John E. Ho. Jr., Reg. No. 18,753, all of Met Telephone Calls to Sande 111 my own knowledge are true are e knowledge that willful false s false statements may jeopardia.	(Status-patented, pendin (Status-patented, pendin (Status-patented, pendin (Status-patented, pendin Inditional transact all business in the Patent and Trade D. Blecker, Reg. No. 29,894; Steven Capella, R. Reg. No. 28,459. H. Daniel Schnurmann, Reg. AL BUSINESS MACHINES CORPORATION: 59. Burton A. Amernick, Reg. No. 24,852. Stan 6: Morris Liss, Reg. No. 24,510. Martin Abran, Reg. No. 32,767, Eric J. Franklin, Reg. No. 3 et. Reg. No. 26,279. Christopher A. Hughes, Reflorgan & Finnegan, L.L.P George Vande Sande Pollock, Vande Sande & Priddy, R. P.O. Box 19088 Washington, D.C. 20036-3425 Und that all statements made on information and be tatements and the like so made are punishable by the text of the application or any patent (Passed) by Scott Flakes	ig, abandoned) g, abandoned) g, abandoned) mark Office connected eg. No. 33.086: Alison No. 35,791. Steven J. Elliott I. Pollock, Reg. ley B. Green, Reg. No. nson, Reg. No. 25.787. 7.134 and Robert Scott eg. No. 26.914. Edward L.L.P. S.A. pelief are believed to be y fine or imprisonment, issued thereon.
I hereby at therewith: D. Morting Soucar, Re No. 16.906 24.351, Ri George R. Wales, Rea A. Penning I hereb true: and fi or both. ur	(U.S. Applicate of the (U.S. Applicate of the (U.S. Applicate oppoint the following Joseph P. Abate, 19 ger. Reg. No. 39,3 g. No. 32,440. Mab. George Vande Schard Wiener, Reg. No. 22 g. No. 39,413; all ogton. Reg. No. 32. Send of sole or first in Signature (U.S.C. § 19 of sole or fi	ion Seria ion Seria ion Seria ing attorm Reg. No 06; Darr irc D. So sande. R g. No. 1 7.369. L of POLL 588: Jos Corresp	defined in 37 CFR eation: al No.) al No. al	(U.S. Filing Date) (U.S. Filing Date) (U.S. Filing Date) to prosecute this application at Ahsan, Reg. No. 32,100: Ira E No. 38,253; Eric W. Petraske. 28,989; all of INTERNATION. obert R. Priddy, Reg. No. 20,16 M. Belser, Jr., Reg. No. 22,95 No. 31,730. Elzbieta Chlopecka ANDE & PRIDDY, John E. Ho. Jr., Reg. No. 18,753, all of M. ort Telephone Calls to: Sande 111 my own knowledge are true are knowledge that willful faises false statements may jeopardicted.	(Status-patented, pendin (Status-patented, pendin (Status-patented, pendin (Status-patented, pendin nd transact all business in the Patent and Trade D. Blecker, Reg. No. 29.894; Steven Capella, R. Reg. No. 28.459. H. Daniel Schnurmann, Reg. AL BUSINESS MACHINES CORPORATION: 69. Burton A. Amernick, Reg. No. 24.852. Stan 66: Morris Liss, Reg. No. 24.510. Martin Abran, Reg. No. 32.767. Eric J. Franklin, Reg. No. 3 el. Reg. No. 26.279. Christopher A. Hughes. Ref. MORGAN & FINNEGAN, L.L.P George Vande Sande Pollock, Vande Sande & Priddy, R.I. P.O. Box 19088 Washington, D.C. 20036–3425 U. ad that all statements made on information and be tatements and the like so made are punishable by the tatements and the like so	ig, abandoned) g, abandoned) g, abandoned) mark Office connected eg. No. 33.086: Alison No. 35,791. Steven J. Elliott I. Pollock, Reg. ley B. Green, Reg. No. nson, Reg. No. 25.787. 7.134 and Robert Scott eg. No. 26.914. Edward L.L.P. S.A. pelief are believed to be y fine or imprisonment, issued thereon.
I hereby ap therewith: D. Morting Soucar, Re No. 16.906 24,351, Ri George R. Wales, Res A. Penning I hereb true: and fi or both. ur Full name Inventor's Residence	(U.S. Applicate of the (U.S. Applicate opoint the following Joseph P. Abate, 19 ger. Reg. No. 39,3 gg. No. 32,440, Mag. George Vande Schard Wiener, Reg. No. 22 gg. No. 39,413; all option. Reg. No. 32. Send Send Send Send Send Send Send Send	ion Seria ion Seria ion Seria ing attorn Reg. No 06; Dar irc D. So iande. R g. No. 1 7.369. L of POLL 588: Joi Corresp statement attements 1001 and	defined in 37 CFR eation: al No.) al No.	(U.S. Filing Date) (U.S. Filing Date) (U.S. Filing Date) to prosecute this application at Ahsan. Reg. No. 32,100: Ira E No. 38,253; Eric W. Petraske. 28,989; all of iNTERNATION. Obert R. Priddy. Reg. No. 20,16 M. Belser. Jr., Reg. No. 22,95 Io. 31,730. Elzbieta Chlopecka ANDE & PRIDDY. John E. Ho. Jr., Reg. No. 18,753, all of Met Telephone Calls to Sande 111 my own knowledge are true are e knowledge that willful false s false statements may jeopardia.	(Status-patented, pendin (Status-patented, pendin (Status-patented, pendin (Status-patented, pendin nd transact all business in the Patent and Trade D. Blecker, Reg. No. 29.894; Steven Capella, R. Reg. No. 28.459. H. Daniel Schnurmann, Reg. AL BUSINESS MACHINES CORPORATION: 69. Burton A. Amernick, Reg. No. 24.852. Stan 66: Morris Liss, Reg. No. 24.510. Martin Abran, Reg. No. 32.767. Eric J. Franklin, Reg. No. 3 el. Reg. No. 26.279. Christopher A. Hughes. Ref. MORGAN & FINNEGAN, L.L.P George Vande Sande Pollock, Vande Sande & Priddy, R.I. P.O. Box 19088 Washington, D.C. 20036–3425 U. ad that all statements made on information and be tatements and the like so made are punishable by the tatements and the like so	ig, abandoned) g, abandoned) g, abandoned) mark Office connected eg. No. 33.086: Alison No. 35,791. Steven J. Elliott I. Pollock, Reg. ley B. Green, Reg. No. nson, Reg. No. 25.787. 7.134 and Robert Scott eg. No. 26.914. Edward L.L.P. S.A. pelief are believed to be y fine or imprisonment, issued thereon.
I hereby at therewith: D. Morting Soucar, Re No. 16.906 24.351, Ri George R. Wales, Res A. Penning I hereb true: and fi or both, un	(U.S. Applicate of the (U.S. Applicate opening the following Joseph P. Abate, 19 ter. Reg. No. 39,3 g. No. 32,440. May George Vande Schard Wiener, Reg. No. 22 g. No. 39,413; all ogton. Reg. No. 32. Send of sole or first important that these stander 18 U.S.C. § 19 of sole or first important and signature Address 2 R. Send Output Ed.	ion Seria ion Seria ion Seria ing attorn Reg. No 06; Darr irc D. So sande. R g. No. 1 7.369. L of POLL 588: Jos Corresp statement atternents 1001 and ventor:	defined in 37 CFR eation: al No.) al No.	(U.S. Filing Date) (U.S. Filing Date) (U.S. Filing Date) to prosecute this application at Ahsan, Reg. No. 32,100: Ira E No. 38,253; Eric W. Petraske. 28,989; all of INTERNATION. obert R. Priddy, Reg. No. 20,16 M. Belser, Jr., Reg. No. 22,95 No. 31,730. Elzbieta Chlopecka ANDE & PRIDDY, John E. Ho. Jr., Reg. No. 18,753, all of M. ort Telephone Calls to: Sande 111 my own knowledge are true are knowledge that willful faises false statements may jeopardicted.	(Status-patented, pendin (Status-patented, pendin (Status-patented, pendin (Status-patented, pendin nd transact all business in the Patent and Trade D. Blecker, Reg. No. 29.894; Steven Capella, R. Reg. No. 28.459. H. Daniel Schnurmann, Reg. AL BUSINESS MACHINES CORPORATION: 69. Burton A. Amernick, Reg. No. 24.852. Stan 66: Morris Liss, Reg. No. 24.510. Martin Abran, Reg. No. 32.767. Eric J. Franklin, Reg. No. 3 el. Reg. No. 26.279. Christopher A. Hughes. Ref. MORGAN & FINNEGAN, L.L.P George Vande Sande Pollock, Vande Sande & Priddy, R.I. P.O. Box 19088 Washington, D.C. 20036–3425 U. ad that all statements made on information and be tatements and the like so made are punishable by the tatements and the like so	ig, abandoned) g, abandoned) g, abandoned) mark Office connected eg. No. 33.086: Alison No. 35,791. Steven J. Elliott I. Pollock, Reg. ley B. Green, Reg. No. nson, Reg. No. 25.787. 7.134 and Robert Scott eg. No. 26.914. Edward L.L.P. S.A. pelief are believed to be y fine or imprisonment, issued thereon.
I hereby ap therewith: D. Morting Soucar, Re No. 16.906 24,351, Ri George R. Wales, Res A. Penning I hereb true: and fi or both. ur Full name Inventor's Residence Citizenship Post Office	(U.S. Applicate of the (U.S. Applicate opoint the following Joseph P. Abate, 19 ger. Reg. No. 39,3 gg. No. 32,440, Mag. George Vande Schard Wiener, Reg. No. 22 gg. No. 39,413; all option. Reg. No. 32. Send Send Send Send Send Send Send Send	ion Seria ion Seria ion Seria ing attorm Reg. No 06; Dar irc D. So lande. R g. No. 1 7.369. L of POLL 588: Joi Corresp Statement attements 1001 and ventor: idde Stat le as	defined in 37 CFR eation: al No.) al No.) levs and/or agents. 30.382; Aziz M. yl K. Neff, Reg. No. leg. No. 17.276, Reg. No. 17.276, Reg. No. 17.276, Reg. No. 17.276, Reg. No. 17.276, Reg. No. 17.276, Reg. No. 17.276, Reg. No. 17.276, Reg. No. 18.741, Townsend 19.00, CK, VANDE Seph C. Redmond. 19.00, CK, VANDE Seph C. Redmond. 19.00, Reg. No.	(U.S. Filing Date) (U.S. Filing Date) (U.S. Filing Date) to prosecute this application at Ahsan, Reg. No. 32,100: Ira E No. 38,253; Eric W. Petraske. 28,989; all of INTERNATION. obert R. Priddy, Reg. No. 20,16 M. Belser, Jr., Reg. No. 22,95 No. 31,730. Elzbieta Chlopecka ANDE & PRIDDY, John E. Ho. Jr., Reg. No. 18,753, all of M. ort Telephone Calls to: Sande 111 my own knowledge are true are knowledge that willful faises false statements may jeopardicted.	(Status-patented, pendin (Status-patented, pendin (Status-patented, pendin (Status-patented, pendin nd transact all business in the Patent and Trade D. Blecker, Reg. No. 29.894; Steven Capella, R. Reg. No. 28.459. H. Daniel Schnurmann, Reg. AL BUSINESS MACHINES CORPORATION: 69. Burton A. Amernick, Reg. No. 24.852. Stan 66: Morris Liss, Reg. No. 24.510. Martin Abran, Reg. No. 32.767. Eric J. Franklin, Reg. No. 3 el. Reg. No. 26.279. Christopher A. Hughes. Ref. MORGAN & FINNEGAN, L.L.P George Vande Sande Pollock, Vande Sande & Priddy, R.I. P.O. Box 19088 Washington, D.C. 20036–3425 U. ad that all statements made on information and be tatements and the like so made are punishable by the tatements and the like so	ig, abandoned) g, abandoned) g, abandoned) mark Office connected eg. No. 33.086: Alison No. 35,791. Steven J. Elliott I. Pollock, Reg. ley B. Green, Reg. No. nson, Reg. No. 25.787. 7.134 and Robert Scott eg. No. 26.914. Edward L.L.P. S.A. pelief are believed to be y fine or imprisonment, issued thereon.

DECLARATION FOR PATENT APPLICATION

Page Two

Inventor's Signature Residence Address Citzenship United States Post Office Address Same as Above Full name of third joint inventor (if any): Inventor's Signature Residence Address 15 Four Winds Drive, Pouchikeeosie, New York 12503 Citzenship Tawan R.O.C. Post Office Address Same as Above Full name of fourth joint inventor (if any): Inventor's Signature Residence Address Citzenship Post Office Address	Fuil name of second joint inventor (if any): Louis L. Hsu	
Citizenship United States Post Office Address Same as Above Full name of third joint inventor (if any): Jence B. Kuang Inventor's Signature Residence Address Citizenship Post Office Address Citizenship Date Contact Citizenship Date Contact Citizenship	Inventor's Signature	Date
Post Office Address Full name of third joint inventor (if any): Full name of third joint inventor (if any): Full name of third joint inventor (if any): Inventor's Signature Residence Address Full name of fourth joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Full name of filth joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Full name of axith joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Citizenship Date Residence Address Citizenship	Residence Address 7 Crosby Court, Fishkill, New York 12524	
Fost Office Address Full name of third joint inventor (if any): Full name of third joint inventor (if any): Full name of third joint inventor (if any): Full name of fibh joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Full name of fibh joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Citizenship Date Residence Address Citizenship Date Residence Address Citizenship Date Residence Address Citizenship	Citizenship <u>United States</u>	
Full name of third joint inventor (if any): Jence B. Kuand Inventor's Signature Date Residence Address 15 Four Winds Drive, Pouchkeepsie, New York 12603 Citizenship Tarvan R.O.C. Post Office Address Same as Above Full name of fourth joint inventor (if any): Inventor's Signature Date Residence Address Full name of fifth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Residence Address Citizenship Date Residence Address Citizenship Citizenship Date Residence Address Citizenship		
Inventor's Signature Date Residence Address 15 Four Winds Drive, Poughkeepsie, New York 12503 Citizenship Tawan ROC. Post Office Address Same as Above Full name of fourth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Citizenship Date Residence Address Citizenship		
Residence Address 15 Four Winds Drive, Pouchkeepsie, New York 12603 Clüzenship Tanwan R.O.C. Post Office Address Same as Above Full name of fourth joint inventor (if any): Inventor's Signature Residence Address Clüzenship Post Office Address Clüzenship Date Residence Address Clüzenship Date Residence Address Clüzenship Date Residence Address Clüzenship	Full name of third joint inventor (if any): Jence B. Kuang	
Citizenship Tarwan ROC. Post Office Address Same as Acove Full name of fourth joint inventor (if any): Inventor's Signature Post Office Address Citizenship Post Office Address Full name of fifth joint inventor (if any): Inventor's Signature Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Full name of sixth joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Citizenship Cutizenship Date Residence Address Citizenship Date Residence Address Citizenship Date Residence Address Citizenship	Inventor's Signature	Date
Post Office Address Same as Above Full name of fourth joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Date Date Residence Address Citizenship Date Residence Address Citizenship Date Residence Address Citizenship		
Post Office Address Same as Above Full name of fourth joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Date Date Residence Address Citizenship Date Residence Address Citizenship Date Residence Address Citizenship	Citizenship Tarwan R.O.C.	
Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of fifth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Citizenship Date Residence Address Citizenship Date Residence Address Citizenship Date Residence Address Citizenship Date Residence Address Citizenship		
Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of fifth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Citizenship Date Residence Address Citizenship Date Residence Address Citizenship Date Residence Address Citizenship Date Residence Address Citizenship		•
Residence Address Citizenship Post Office Address Full name of fifth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of sixth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Residence Address Citizenship Date Residence Address Citizenship Rost Office Address Citizenship Date Residence Address Citizenship Date Residence Address Citizenship	Fuil name of tourth joint inventor (if any):	
Citizenship Post Office Address Full name of fifth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of sixth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Residence Address Citizenship Date Residence Address Citizenship Date Residence Address Citizenship	Inventor's Signature	Date
Post Office Address Full name of fifth joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Full name of sixth joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Date Residence Address Citizenship Date Date Residence Address Citizenship Date Residence Address Citizenship Date Residence Address Citizenship	Residence Address	
Full name of fifth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Citizenship Date Residence Address Citizenship Date Citizenship Citizenship	Citizenship	
Inventor's Signature	Post Office Address	
Inventor's Signature		
Residence Address Citizenship Post Office Address Full name of sixth joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Full name of eighth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Date Residence Address		
Citizenship Post Office Address Full name of sixth joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Citizenship Post Office Address Full name of eighth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship		
Post Office Address Full name of sixth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of eighth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of eighth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship		
Full name of sixth joint inventor (if any): Inventor's Signature		
Inventor's Signature	Post Office Address	
Inventor's Signature		
Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of eighth joint inventor (if any): Inventor's Signature Date Citizenship Citizenship Date Residence Address Citizenship		
Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of eighth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Citizenship Citizenship		
Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of eighth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship		
Full name of seventh joint inventor (if any): Inventor's Signature Date Residence Address Citizenship Post Office Address Full name of eighth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship		
Inventor's Signature	Post Office Address	
Inventor's Signature	Full name of seventh joint inventor (if any):	
Residence Address Citizenship Post Office Address Full name of eighth joint inventor (if any): Inventor's Signature Residence Address Citizenship		Date
Citizenship Post Office Address Full name of eighth joint inventor (if any): Inventor's Signature Residence Address Citizenship		
Post Office Address Full name of eighth joint inventor (if any): Inventor's Signature Date Residence Address Citizenship		
Full name of eighth joint inventor (if any): Inventor's Signature		
Inventor's Signature Date	1 001 CANOD - INDICATE -	
Inventor's Signature Date	Full name of eighth joint inventor (if any):	
Residence Address		Date
Citizenship		

ı
M
a
:=
-
123
1

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

	claimed and for which a par	tent is sought on the invention		are listed below)
	CIRCUIT AND METH	IODS TO IMPROVE THE OP	ERATION OF SOI DEVICES	
the specification of which: (ch	neck one)			
[XX] is attached hereto.	[] was filed on		t Application Serial No. or PCT International Ap 19 (if applicable).	plication Number
I hereby state that I have re referred to above.	viewed and understand the o	contents of the above-identified	specification, including the claims, as amended by	y any amendment
Prior Foreign Application(s inventor's certificate listed below	s): I hereby claim foreign proow, or § 365(a) of any PC7	riority benefits under 35 U.S.C. international application which	of this application in accordance with 37 CFR § \$119(a)-(d) or §365(b) of any foreign applicant the designated at least one country other than the eventor's certificate having a filing date before that	on(s) for patent or United States of
				Priority Claimed
(Application No.)	-	(Country)	(Day/Month/Year Filed)	Yes Vo
(Application No.)		(Country)	(Day/Month/Year Filed)	[] [] Yes No
(Application No.)	-	(Country)	(Day/Month/Year Filed)	[] [] Yes No
I hereby claim the benefit	under Title 35. United State	s Code § 119(e) of any United	States provisional application(s) listed below:	
	Application No. 60/044.251		Filing Date April 23, 1997	
(U.S. Application		(U.S. Filing Date)	(Status—patented, pending, ab	andoned)
		((Status-patented, pending, ao	
therewith: Joseph P. Abate. Re D. Mortinger, Reg. No. 39,306 Soucar, Reg. No. 32,440, Marc No. 16,906. George Vande Sar 24,351, Richard Wiener, Reg. George R. Pettit, Reg. No. 27,3	attorneys and/or agents to p.g. No. 30.382; Aziz M. Ah. 5; Daryl K. Neff, Reg. No. D. Schechter, Reg. No. 28, ide, Reg. No. 17.276, Robei No. 18.741, Townsend M. 369, Louis Woo, Reg. No. 2 POLLOCK, VANDE SANI	(U.S. Filing Date) prosecute this application and to san. Reg. No. 32.100: Ira D E 38.253; Eric W. Petraske. Reg. 989: all of INTERNATIONAL at R. Priddy. Reg. No. 20.169. Belser, Jr., Reg. No. 22.956; March 1988; Belser, Jr., Reg. No. 22.956; March 200; PRIDDY; John E. Hoel, DE & PRIDDY; John E. Hoel,	(Statuspatented, pending, ab ransact all business in the Patent and Trademark lecker. Reg. No. 29.894; Steven Capella, Reg. No. 28,459, H. Daniel Schnurmann, Reg. No. BUSINESS MACHINES CORPORATION; Ellic Burton A. Amernick, Reg. No. 24,352, Stanley B Morris Liss, Reg. No. 24,510, Martin Abramson, eg. No. 32,767, Eric J. Franklin, Reg. No. 37,134 Reg. No. 26,279, Christopher A. Hughes, Reg. No.	andoned) Office connected Io. 33.086; Alison 35.791, Steven J. ott I. Pollock, Reg. B. Green, Reg. No. Reg. No. 25.787. And Robert Scott
I hereby appoint the following therewith: Joseph P. Abate. Re D. Mortinger, Reg. No. 39,306 Soucar, Reg. No. 32,440, Marc No. 16,906. George Vande Sar 24,351, Richard Wiener, Reg. George R. Pettit. Reg. No. 27,3 Wales, Reg. No. 39,413; all of A. Pennington, Reg. No. 32,58	attorneys and/or agents to p.g. No. 30.382; Aziz M. Ah. 5; Daryl K. Neff, Reg. No. D. Schechter, Reg. No. 28, ide, Reg. No. 17.276, Robei No. 18.741, Townsend M. 369, Louis Woo, Reg. No. 2 POLLOCK, VANDE SANI	(U.S. Filing Date) prosecute this application and to san. Reg. No. 32.100: Ira D E 38.253; Eric W. Petraske, Reg. 989: all of INTERNATIONAL et R. Priddy, Reg. No. 20.169. Belser, Jr., Reg. No. 22.956; No. 31,730, Elzbieta Chlopecka, Reg. PRIDDY; John E. Hoel, Reg. No. 18.753: all of MOR relephone Calls to:	(Statuspatented, pending, ab ransact all business in the Patent and Trademark lecker. Reg. No. 29.894; Steven Capella, Reg. No. 28,459, H. Daniel Schnurmann. Reg. No. BUSINESS MACHINES CORPORATION; Ellic Burton A. Amernick, Reg. No. 24.852, Stanley B Morris Liss, Reg. No. 24.510, Martin Abramson. eg. No. 32,767, Eric J. Franklin. Reg. No. 37,134 Reg. No. 26,279, Christopher A. Hughes. Reg. No. George Vande Sande Pollock, Vande Sande & Priddy, R.L.L.P. P.O. Box 19088	andoned) Office connected Jo. 33.086; Alison 35.791, Steven J. ott I. Pollock, Reg. Green, Reg. No. Reg. No. 25.787. and Robert Scott o. 26.914, Edward
I hereby appoint the following therewith: Joseph P. Abate. Re D. Mortinger, Reg. No. 39,306 Soucar, Reg. No. 32,440, Marc No. 16,906. George Vande Sar 24,351, Richard Wiener, Reg. George R. Pettit, Reg. No. 27,3 Wales, Reg. No. 39,413; all of A. Pennington, Reg. No. 32,58 Send C	attorneys and/or agents to p. g. No. 30.382; Aziz M. Ah. 5; Daryl K. Neff, Reg. No. 28. de, Reg. No. 17.276, Rober No. 18.741, Townsend M. 369, Louis Woo, Reg. No. 37.276, POLLOCK, VANDE SANI 38; Joseph C. Redmond, Jr. orrespondence and Direct T. George Vande San (202) 331-7111 attements made herein of myements are made with the kn	(U.S. Filing Date) prosecute this application and to san, Reg. No. 32.100; Ira D E 38.253; Eric W. Petraske, Reg. 989; all of INTERNATIONAL at R. Priddy, Reg. No. 20.169. Belser, Jr., Reg. No. 22.956; No. 31,730, Elzbieta Chlopecka, Reg. No. 18.753; all of MOF delephone Calls to: de	(Statuspatented, pending, ab ransact all business in the Patent and Trademark lecker. Reg. No. 29.894; Steven Capella, Reg. No. 28,459, H. Daniel Schnurmann. Reg. No. BUSINESS MACHINES CORPORATION; Ellic Burton A. Amernick, Reg. No. 24.852, Stanley B Morris Liss, Reg. No. 24.510, Martin Abramson. eg. No. 32,767, Eric J. Franklin, Reg. No. 37,134 Reg. No. 26,279, Christopher A. Hughes, Reg. No. George Vande Sande Pollock, Vande Sande & Priddy, R.L.L.P.	andoned) Office connected to. 33.086; Alison 35.791, Steven J. ott I. Pollock, Reg. B. Green, Reg. No. Reg. No. 25.787. A and Robert Scott o. 26.914, Edward Tare believed to be e or imprisonment.
I hereby appoint the following therewith: Joseph P. Abate. Re D. Mortinger, Reg. No. 39,306 Soucar, Reg. No. 32,440, Marc No. 16,906. George Vande Sar 24,351, Richard Wiener, Reg. George R. Pettit, Reg. No. 27,3 Wales, Reg. No. 39,413; all of A. Pennington, Reg. No. 32,58 Send C	attorneys and/or agents to p. g. No. 30.382; Aziz M. Ah. 5; Daryl K. Neff, Reg. No. 28. de, Reg. No. 17.276, Rober No. 18.741, Townsend M. 369, Louis Woo, Reg. No. 3POLLOCK, VANDE SANI 38; Joseph C. Redmond, Jr. orrespondence and Direct T George Vande San (202) 331-7111 attements made herein of my ements are made with the kn 01 and that such willful false.	(U.S. Filing Date) prosecute this application and to san, Reg. No. 32.100; Ira D E 38.253; Eric W. Petraske, Reg. 989; all of INTERNATIONAL at R. Priddy, Reg. No. 20.169. Belser, Jr., Reg. No. 22.956; No. 31,730, Elzbieta Chlopecka, Reg. No. 18.753; all of MOF delephone Calls to: de	(Statuspatented, pending, ab ransact all business in the Patent and Trademark lecker. Reg. No. 29.894; Steven Capella, Reg. No. 28.459, H. Daniel Schnurmann. Reg. No. BUSINESS MACHINES CORPORATION; Ellic Burton A. Amernick, Reg. No. 24.352, Stanley B Morris Liss, Reg. No. 24.510, Martin Abramson. eg. No. 32.767, Eric J. Franklin, Reg. No. 37,134 Reg. No. 26,279, Christopher A. Hughes, Reg. No. George Vande Sande Pollock, Vande Sande & Priddy, R.L.L.P. P.O. Box 19088 Washington, D.C. 20036-3425 U.S.A. nat all statements made on information and belief ments and the like so made are punishable by fine the validity of the application or any patent issue.	andoned) Office connected to. 33.086; Alison 35.791, Steven J. ott I. Pollock, Reg. B. Green, Reg. No. Reg. No. 25.787. A and Robert Scott o. 26.914, Edward Tare believed to be e or imprisonment.
I hereby appoint the following therewith: Joseph P. Abate. Re D. Mortinger, Reg. No. 39,306 Soucar, Reg. No. 32,440, Marc No. 16,906. George Vande Sar 24,351, Richard Wiener, Reg. George R. Pettit. Reg. No. 27,3 Wales. Reg. No. 39,413; all of A. Pennington, Reg. No. 32,58 Send C I hereby declare that all statrue; and further that these state or both, under 18 U.S.C. § 10 Full name of sole or first in (heir)	attorneys and/or agents to p. g. No. 30.382; Aziz M. Ah. 6; Daryl K. Neff, Reg. No. 28. de. Reg. No. 17.276, Rober No. 18.741, Townsend M. 369, Louis Woo, Reg. No. 369, Louis Woo, Reg. No. 37.276, Vande Sani (202) 331-7111 attements made herein of my ements are made with the knot and that such willful false ventor: Roy Chil	(U.S. Filing Date) prosecute this application and to san. Reg. No. 32.100: Ira D E 38.253; Eric W. Petraske, Reg 989; all of INTERNATIONAL At R. Priddy, Reg. No. 20.169. Belser, Jr., Reg. No. 22.956; No. 1730, Elzbieta Chlopecka, Robe & PRIDDY; John E. Hoel, Reg. No. 18.753; all of MOF delephone Calls to: de own knowledge are true and thouledge that willful false states statements may jeopardize to the control of the cont	(Statuspatented, pending, ab ransact all business in the Patent and Trademark lecker. Reg. No. 29.894; Steven Capella, Reg. No. 28.459, H. Daniel Schnurmann. Reg. No. BUSINESS MACHINES CORPORATION; Ellic Burton A. Amernick, Reg. No. 24.352, Stanley B Morris Liss, Reg. No. 24.510, Martin Abramson. eg. No. 32.767, Eric J. Franklin, Reg. No. 37,134 Reg. No. 26,279, Christopher A. Hughes, Reg. No. George Vande Sande Pollock, Vande Sande & Priddy, R.L.L.P. P.O. Box 19088 Washington, D.C. 20036-3425 U.S.A. nat all statements made on information and belief ments and the like so made are punishable by fine the validity of the application or any patent issue.	andoned) Office connected to 33.086; Alison 35.791, Steven J. ott I. Pollock, Reg. 8. Green, Reg. No. Reg. No. 25.787. 4 and Robert Scott o. 26.914, Edward
I hereby appoint the following therewith: Joseph P. Abate. Re D. Mortinger, Reg. No. 39,306 Soucar, Reg. No. 32,440, Marc No. 16,906. George Vande Sar 24,351, Richard Wiener, Reg. George R. Pettit. Reg. No. 27,3 Wales. Reg. No. 39,413; all of A. Pennington, Reg. No. 32,58 Send C	attorneys and/or agents to p. g. No. 30.382; Aziz M. Ah. 6; Daryl K. Neff, Reg. No. 28. de, Reg. No. 17.276, Rober No. 18.741, Townsend M. 369, Louis Woo, Reg. No. 38; Joseph C. Redmond. Jr. orrespondence and Direct T George Vande San (202) 331-7111 attements made herein of my ements are made with the kn 01 and that such willful false ventor: Roy Chill	(U.S. Filing Date) prosecute this application and to san. Reg. No. 32.100: Ira D B 38.253; Eric W. Petraske. Reg 989: all of INTERNATIONAL at R. Priddy. Reg. No. 20.169. Belser, Jr., Reg. No. 22.956; No. 31,730, Elzbieta Chlopecka. Red & PRIDDY; John E. Hoel, Reg. No. 18.753: all of MOF delephone Calls to: de count knowledge are true and the lowledge that willful false state se statements may jeopardize the count of t	(Status—patented, pending, ab ransact all business in the Patent and Trademark lecker. Reg. No. 29.894; Steven Capella, Reg. No. 28,459, H. Daniel Schnurmann. Reg. No. BUSINESS MACHINES CORPORATION; Ellic Burton A. Amernick, Reg. No. 24.852, Stanley B Morris Liss, Reg. No. 24.510, Martin Abramson. eg. No. 32,767, Eric J. Franklin, Reg. No. 37,134 Reg. No. 26,279, Christopher A. Hughes, Reg. No. George Vande Sande Pollock, Vande Sande & Priddy, R.L.L.P. P.O. Box 19088 Washington, D.C. 20036—3425 U.S.A. nat all statements made on information and belief ments and the like so made are punishable by fine he validity of the application or any patent issue.	andoned) Office connected to 33.086; Alison 35.791, Steven J. ott I. Pollock, Reg. 8. Green, Reg. No. Reg. No. 25.787. 4 and Robert Scott o. 26.914, Edward
I hereby appoint the following therewith: Joseph P. Abate. Re D. Mortinger, Reg. No. 39,306 Soucar, Reg. No. 32,440, Marc No. 16,906. George Vande Sar 24,351, Richard Wiener, Reg. George R. Pettit, Reg. No. 27,3 Wales. Reg. No. 39,413; all of A. Pennington, Reg. No. 32,58 Send Co. I hereby declare that all statrue; and further that these state or both, under 18 U.S.C. § 100 Full name of sole or first in (heir) Inventor's Signature Residence Address 2 Richard	attorneys and/or agents to p. g. No. 30.382; Aziz M. Ah. 5; Daryl K. Neff. Reg. No. 28. de, Reg. No. 17.276, Rober No. 18.741, Townsend M. 369, Louis Woo, Reg. No. 38; Joseph C. Redmond. Jr. orrespondence and Direct T. George Vande San (202) 331-7111 attements made herein of my ements are made with the kn 01 and that such willful false ventor: Roy Chilled Road, Ess	(U.S. Filing Date) prosecute this application and to san. Reg. No. 32.100: Ira D B 38.253; Eric W. Petraske. Reg 989: all of INTERNATIONAL at R. Priddy. Reg. No. 20.169. Belser, Jr., Reg. No. 22.956; No. 31,730, Elzbieta Chlopecka. Red & PRIDDY; John E. Hoel, Reg. No. 18.753: all of MOF delephone Calls to: de count knowledge are true and the lowledge that willful false state se statements may jeopardize the count of t	(Status—patented, pending, ab ransact all business in the Patent and Trademark lecker. Reg. No. 29.894; Steven Capella, Reg. No. 28,459, H. Daniel Schnurmann. Reg. No. BUSINESS MACHINES CORPORATION; Ellic Burton A. Amernick, Reg. No. 24.852, Stanley B Morris Liss, Reg. No. 24.510, Martin Abramson. eg. No. 32,767, Eric J. Franklin, Reg. No. 37,134 Reg. No. 26,279, Christopher A. Hughes, Reg. No. George Vande Sande Pollock, Vande Sande & Priddy, R.L.L.P. P.O. Box 19088 Washington, D.C. 20036—3425 U.S.A. nat all statements made on information and belief ments and the like so made are punishable by fine he validity of the application or any patent issue.	andoned) Office connected to 33.086; Alison 35.791, Steven J. ott I. Pollock, Reg. 8. Green, Reg. No. Reg. No. 25.787. 4 and Robert Scott o. 26.914, Edward
I hereby appoint the following therewith: Joseph P. Abate. Re D. Mortinger, Reg. No. 39,306 Soucar, Reg. No. 32,440, Marc No. 16,906. George Vande Sar 24,351, Richard Wiener, Reg. George R. Pettit. Reg. No. 27,3 Wales. Reg. No. 39,413; all of A. Pennington, Reg. No. 32,58 Send C	attorneys and/or agents to p. g. No. 30.382; Aziz M. Ah. 6; Daryl K. Neff, Reg. No. 10. Schechter, Reg. No. 28. de. Reg. No. 17.276, Rober No. 18.741, Townsend M. 369, Louis Woo, Reg. No. 369, Louis Woo, Reg. No. 37. POLLOCK, VANDE SANI 38; Joseph C. Redmond. Jr. orrespondence and Direct T George Vande San (202) 331-7111 attements made herein of my ements are made with the knool and that such willful false ventor: Roy Chilled Road, Essible Calles	(U.S. Filing Date) prosecute this application and to san. Reg. No. 32.100: Ira D B 38.253; Eric W. Petraske. Reg 989: all of INTERNATIONAL at R. Priddy. Reg. No. 20.169. Belser, Jr., Reg. No. 22.956; No. 31,730, Elzbieta Chlopecka. Red & PRIDDY; John E. Hoel, Reg. No. 18.753: all of MOF delephone Calls to: de count knowledge are true and the lowledge that willful false state se statements may jeopardize the count of t	(Status—patented, pending, ab ransact all business in the Patent and Trademark lecker. Reg. No. 29.894; Steven Capella, Reg. No. 28,459, H. Daniel Schnurmann. Reg. No. BUSINESS MACHINES CORPORATION; Ellic Burton A. Amernick, Reg. No. 24.852, Stanley B Morris Liss, Reg. No. 24.510, Martin Abramson. eg. No. 32,767, Eric J. Franklin, Reg. No. 37,134 Reg. No. 26,279, Christopher A. Hughes, Reg. No. George Vande Sande Pollock, Vande Sande & Priddy, R.L.L.P. P.O. Box 19088 Washington, D.C. 20036—3425 U.S.A. nat all statements made on information and belief ments and the like so made are punishable by fine he validity of the application or any patent issue.	andoned) Office connected to 33.086; Alison 35.791, Steven J. ott I. Pollock, Reg. 8. Green, Reg. No. Reg. No. 25.787. 4 and Robert Scott o. 26.914, Edward

Page Two

Full name of second joint inventor (if any): Louis L. Hsu	
Inventor's Signature	Date
Residence Address 7 Crosby Court, Fishkill, New York 12524	
Citizenship <u>United States</u>	
Post Office Address Same as Above	
Full name of third joint inventor (if any): <u>Jente B. Kuang</u>	
Inventor's Signature	Date
Residence Address 15 Four Winds Drive, Poughkeepsie, New York	12603
Citizenship Taiwan R.O.C.	
Post Office Address Same as Above	
Full name at fourth court inventor (if any):	
Fuil name of fourth joint inventor (if any): Inventor's Signature	Data
Residence Address	Date
Citizenship	
Post Office Address	
Full name of fifth joint inventor (if any):	
inventor's Signature	Date
Residence Address	
Citizenship	
Post Office Address	
Full name of sixth joint inventor (if any):	
Inventor's Signature	Date
Residence AddressCitizenship	
CitizenshipPost Office Address	
Full name of seventh joint inventor (if any):	
Inventor's Signature	Date
Residence Address	
Citizenship	
Post Office Address	
Full name of eighth joint inventor (if any):	
Inventor's Signature	Date
Residence Address	
Citizenship	
Ost Office Address	

As a below-named inventor, I hereby declare that:

My residence, post office address and cittzenship are as stated below next to my name.

		only one name is listed below) or an patent is sought on the invention en	original, first and joint inventor (if plural namutiled:	nes are listed below)
	CIRCUIT AND ME	THODS TO IMPROVE THE OPER	LATION OF SOI DEVICES	
the specification of which: (ch	neck one)			
[XX] is attached hereto.	was filed on		Application Serial No or PCT International . 19 (if applicable).	Application Number
I hereby state that I have referred to above.	viewed and understand th	e contents of the above-identified sp	ecification, including the claims, as amended	i by any amendment
Prior Foreign Application(s inventor's certificate listed bel	s): I hereby claim foreign ow, or § 365(a) of any P	priority benefits under 35 U.S.C. § CT international application which	f this application in accordance with 37 CFR 119(a)-(d) or \$365(b) of any foreign applicates designated at least one country other than emor's certificate having a filling date before the	ation(s) for patent or the United States of nat of the application
	_			Priority Claimed
(Application No.)		(Country)	(Day/Month/Year Filed)	Yes No
(Application No.)		(Country)	(Day/Month/Year Filed)	[] [] Yes No
(Application No.)	-	(Country)	(Day/Month/Year Filed)	[][] Yes No
I hereby claim the benefit	under Title 35, United St	ates Code § 119(e) of any United S	States provisional application(s) listed below	:
	Application No. 60/044.251		Filing Date April 23, 1997	
(U.S. Application		(U.S. Filing Date)	(Statuspatented, pending,	abandoned)
(U.S Application	n Serial Vo.)	(U.S. Filing Date)	(Status-patented, pending,	abandoned)
therewith: Joseph P Abate, Re D. Mortinger, Reg. No. 39,306 Soucar, Reg. No. 32,440, Marc No. 16,906. George Vande Sar 24,351. Richard Wiener, Reg. George R. Pettit, Reg. No. 27,2 Wales, Reg. No. 39,413; all of	g. No. 30,382; Aziz M. 6; Daryi K. Neff, Reg. No. 2 D. Schechter, Reg. No. 2 Ide, Reg. No. 17,276, Rol No. 18,741, Townsend No. 369, Louis Woo, Reg. No. POLLOCK, VANDE SA	Ahsan, Reg. No. 32.100: Ira D. Ble D. 38.253; Eric W Petraske, Reg. 1 8.989; all of INTERNATIONAL Bi- bert R. Priddy, Reg. No. 20.169, Bu M. Belser, Jr., Reg. No. 22.956; Mo D. 31.730, Elzbieta Chlopecka, Reg.	nsact all business in the Patent and Trademacker, Reg. No. 29.894; Steven Capella, Reg. No. 28.459, H. Daniel Schnurmann, Reg. N USINESS MACHINES CORPORATION; Einton A. Amernick, Reg. No. 24.852, Stanley oris Liss, Reg. No. 24.510, Martin Abramso, No. 32.767, Eric J. Franklin, Reg. No. 37.1 g. No. 26.279, Christopher A. Hughes, Reg. AN & FINNEGAN, L.L.P	No. 33.086: Alison to. 35.791. Steven J. Hiott I. Pollock, Reg. B. Green, Reg. No. on, Reg. No. 25.787. 34 and Robert Scott
Send C	orrespondence and Direct	: Telephone Calls to:	George Vande Sande	
	George Vande S (202) 331-711		Pollock, Vande Sande & Priddy, R.L.L P.O. Box 19088	P.
			Washington, D.C. 20036-3425 U.S.	
true; and further that these state	ments are made with the	knowledge that willful false statement	all statements made on information and belients and the like so made are punishable by f validity of the application or any patent issues.	ine or imprisonment.
Full name of sole or first inver	ntor: Roy Child	ls Flaker (deceas	sed) by Bruce Flaker	(heir)
Inventor's Signature X 130	we Thehe		Date 3 4/7/	
Residence Address 2 Ric	dge Road, Es	sex Junction, Ve	rmont 05452	
Citizenship United S				
Post Office Address Same				

Page Two

Full name of second joint inventor (if any): Louis L. Hsu	
Inventor's Signature	
Residence Address 7 Crosby Court, Fishkill, New York 12524	
Citizenship <u>United States</u>	
Post Office Address Same as Above	
Full name of third joint inventor (if any): Jente B. Kuang	
Inventor's Signature	
Residence Address 15 Four Winds Drive, Poughkeepsie, New York	12603
Citizenship Taiwan R.O.C.	
Post Office Address Same as Above	
Full name of fourth joint inventor (if any):	
Inventor's Signature	
Resigence Address	
Citizenship	
Post Office Address	
Full name of fifth joint inventor (if any):	
Inventor's Signature	
Residence Address	
Citizenship	
Post Office Address	
Full name of sixth joint inventor (if any): Inventor's Signature	Date
Residence Address	
Citizenship	
Post Office Address	
Full name of seventh joint inventor (if any):	
Inventor's Signature	Date
Residence Address	
Citizenship	
Post Office Address	
Full name of eighth joint inventor (if any):	
Inventor's Signature	
Residence Address	
Citizenship	
Post Office Address	

As a below-named inventor. I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a parent is sought on the invention entitled:

the specification of which: (check or	ne)			
[XX] is attached hereto.	was filed on		nt Application Serial No. or PCT International 19 (if applicable).	Application Number
I hereby state that I have reviewed referred to above.	d and understand the c	ontents of the above-identified	t specification, including the claims, as amende	d by any amendment
Prior Foreign Application(s): I he inventor's certificate listed below, or	ereby claim foreign pr § 365(a) of any PCT	iority benefits under 35 U.S.C international application whi	of this application in accordance with 37 CF. § 119(a)-(d) or §365(b) of any foreign application designated at least one country other than inventor's certificate having a filing date before	cation(s) for patent or the United States of
				Priority Claimed
(Application No.)	-	(Country)	(Day/Month/Year Filed)	[] [] Yes No
(Application No.)	-	(Country)	(Day/Month/Year Filed)	[] [] Yes No
(Application No.)	-	(Country)	(Day/Month/Year Filed)	[] [] Yes No
I hereby claim the benefit under	Title 35, United State	s Code § 119(e) of any Unite	ed States provisional application(s) listed below	w;
	Application No 60/044 251		Filing Date April 23, 1997	
to disclose material information as de	etined in 37 CFR § 1		ovided by 35 U.S.C. § 112, first paragraph, I are the filling date of the prior application and	_
• •	etined in 37 CFR § 1 ation:			the national or PC7
(U.S. Application Serial Information as de international filing date of this application Serial (U.S. Application Serial (U.S. Application Serial Information Info	etined in 37 CFR § 1 ation: I No.) eys and/or agents to p. 30.382; Aziz M. Ahs. I K. Neff, Reg. No. 3. hechter, Reg. No. 28.9 g. No. 17,276, Rober 3,741, Townsend M. 1 ouis Woo, Reg. No. 30 OCK, VANDE SAND	(U.S. Filing Date) (U.S. Filing Date) (U.S. Filing Date) (U.S. Filing Date) prosecute this application and san, Reg. No. 32,100: Ira D. I. 38,253: Eric W. Petraske, Reg. 89; all of INTERNATIONAL tr. R. Priddy. Reg. No. 20,169, Belser, Jr., Reg. No. 22,956; 11,730, Elzbieta Chlopecka, R. DE & PRIDDY: John E. Hoel,	(Statuspatented, pending (Statuspatented, pending transact all business in the Patent and Tradem Blecker, Reg. No. 29.894: Steven Capella, Reg. No. 28,459. H. Daniel Schnurmann, Reg. No. BUSINESS MACHINES CORPORATION: Burton A. Amernick, Reg. No. 24.852. Stanle Morris Liss, Reg. No. 24.510. Martin Abrams Reg. No. 32,767, Eric J. Franklin, Reg. No. 37. Reg. No. 26,279, Christopher A. Hughes, Reg.	abandoned) abandoned) ark Office connected No. 33.086. Alison No. 35.791. Steven J Elliott I. Pollock, Reg by B. Green, Reg. No. 25,787 134 and Robert Scot
(U.S. Application Serial I hereby appoint the following attornetherewith: Joseph P. Abate. Reg. No. D. Mortinger. Reg. No. 39,306; Dary Soucar. Reg. No. 32,440. Marc D. Sch No. 16,906. George Vande Sande. Reg. 4,351, Richard Wiener, Reg. No. 18 George R. Pettit, Reg. No. 27,369. Low Wales. Reg. No. 39,413; all of POLLO A. Pennington. Reg. No. 32,588; Joseph 19, 200 (19,25).	etined in 37 CFR § 1 ation: I No.) eys and/or agents to p. 30.382; Aziz M. Ahs. I K. Neff, Reg. No. 3. hechter, Reg. No. 28.9 g. No. 17,276, Rober 3,741, Townsend M. 1 ouis Woo, Reg. No. 30 OCK, VANDE SAND	(U.S. Filing Date) (U.S. Filing Date) (U.S. Filing Date) (U.S. Filing Date) prosecute this application and san, Reg. No. 32,100: Ira D. I. 38,253: Eric W. Petraske, Reg. 289; all of INTERNATIONAL tr. R. Priddy. Reg. No. 20,169, Belser, Jr., Reg. No. 22,956; 11,730, Elzbieta Chlopecka, R. DE & PRIDDY; John E. Hoel, Reg. No. 18,753: all of MOI elephone Calls to:	(Statuspatented, pending (Statuspatented, pending transact all business in the Patent and Tradem Blecker, Reg. No. 29.894: Steven Capella, Reg. No. 28,459. H. Daniel Schnurmann, Reg. N. BUSINESS MACHINES CORPORATION: I Burton A. Amernick, Reg. No. 24.852. Stanle Morris Liss, Reg. No. 24.510. Martin Abrams Reg. No. 32,767, Eric J. Franklin, Reg. No. 37. Reg. No. 26,279, Christopher A. Hughes, Reg RGAN & FINNEGAN, L.L.P George Vande Sande Pollock, Vande Sande & Priddy, R.L. P.O. Box 19088	abandoned) abandoned) ark Office connecte No. 33.086. Aliso No. 35.791. Steven Elliott I. Pollock. Reg. No. 95.787. And Robert Sco. No. 26.914. Edwar L.P.
(U.S. Application Seria I hereby appoint the following attornetherewith: Joseph P. Abate. Reg. No. D. Mortinger. Reg. No. 39,306; Dary Soucar. Reg. No. 32,440. Marc D. Sch No. 16,906, George Vande Sande. Re 24,351, Richard Wiener, Reg. No. 27,369. Low Wales. Reg. No. 39,413; all of POLLO A. Pennington. Reg. No. 32,588; Joseph Corresponding to the policy of the polic	etined in 37 CFR § 1 ation: d No.) eys and/or agents to p 30.382; Aziz M. Ans etil K. Neff, Reg. No. 28.5 g. No. 17,276, Rober 3,741, Townsend M. 2 cours Woo, Reg. No. 3 OCK, VANDE SAND eph C. Redmond, Jr., ondence and Direct T George Vande Sand (202) 331-7111 ts made herein of my are made with the kn	(U.S. Filing Date) (I.S.	(Statuspatented, pending (Statuspatented, pending transact all business in the Patent and Tradem Blecker, Reg. No. 29.894: Steven Capella, Reg. No. 28,459. H. Daniel Schnurmann, Reg. No. BUSINESS MACHINES CORPORATION: I Burton A. Amernick, Reg. No. 24.852. Stanle Morris Liss, Reg. No. 24.510. Martin Abrams Reg. No. 32,767, Eric J. Franklin, Reg. No. 37. Reg. No. 26,279, Christopher A. Hughes, Reg RGAN & FINNEGAN, L.L.P George Vande Sande Pollock, Vande Sande & Priddy, R.L.	i the national or PCT, abandoned) abandoned) ark Office connected of the policy of t
(U.S. Application Seria (U.S. Application Ser	etined in 37 CFR § 1 attorn: d No.) d No.) eys and/or agents to p 30.382; Azız M. Ahsyl K. Neff, Reg. No. 28.5 g. No. 17,276. Rober 8,741, Townsend M. 200CK, VANDE SAND eph C. Redmond, Jr., ondence and Direct T George Vande Sand (202) 331-7111 gs made herein of my are made with the knit that such willful fals	(U.S. Filing Date) (U.S. Filing Date) (U.S. Filing Date) (U.S. Filing Date) prosecute this application and san, Reg. No. 32,100: Ira D. It 38,253: Eric W. Petraske, Reg. 289; all of INTERNATIONAL at R. Priddy. Reg. No. 20,169, Belser, Jr., Reg. No. 22,956; 11,730. Elzbieta Chlopecka, R. DE & PRIDDY; John E. Hoel, Reg. No. 18,753: all of MOI elephone Calls to: ide own knowledge are true and to owledge that willful false state e statements may jeopardize in Flaker (dece	(Statuspatented, pending (Statuspatented, pending (Statuspatented, pending transact all business in the Patent and Tradem Blecker, Reg. No. 29.894: Steven Capella, Reg. No. 28,459. H. Daniel Schnurmann, Reg. N. BUSINESS MACHINES CORPORATION: I Burton A. Amernick, Reg. No. 24.852. Stanle Morris Liss, Reg. No. 24.510. Martin Abrams leg. No. 32,767, Eric J. Franklin, Reg. No. 37. Reg. No. 26,279, Christopher A. Hughes, Reg. RGAN & FINNEGAN, L.L.P George Vande Sande Pollock, Vande Sande & Priddy, R.L. P.O. Box 19088 Washington, D.C. 20036-3425 U.Statal statements made on information and be ements and the like so made are punishable by the validity of the application or any patent is	abandoned) abandoned) ark Office connected of the conne
(U.S. Application Seria I hereby appoint the following attornetherewith: Joseph P. Abate, Reg. No. D. Mortinger, Reg. No. 39,306; Dary Soucar, Reg. No. 32,440, Marc D. Sch No. 16,906, George Vande Sande, Re 24,351, Richard Wiener, Reg. No. 18 George R. Pettit, Reg. No. 27,369, Lo Wales, Reg. No. 39,413; all of POLLO A. Pennington, Reg. No. 32,588; Joseph Corresponding to the control of the con	etined in 37 CFR § 1 ation: I No.) INO.) eys and/or agents to p 30.382; Aziz M. Ahs IV K. Neff, Reg. No. 28.9 in the chier, Reg. No. 28.9 in the chier, Reg. No. 28.9 in the chier, Reg. No. 30 CK, VANDE SAND eph C. Redmond, Jr., ondence and Direct T George Vande Sand (202) 331-7111 is made herein of my are made with the kill that such willful fals	(U.S. Filing Date) (I.S. Assistance of the possession of	(Statuspatented, pending (Statuspatented, pending (Statuspatented, pending transact all business in the Patent and Tradem Blecker, Reg. No. 29.894: Steven Capella, Reg. No. 28,459. H. Daniel Schnurmann, Reg. No. BUSINESS MACHINES CORPORATION: I Burton A. Amernick, Reg. No. 24.852. Stanle Morris Liss, Reg. No. 24.510. Martin Abrams Reg. No. 32,767, Eric J. Franklin, Reg. No. 37. Reg. No. 26,279, Christopher A. Hughes, Reg. RGAN & FINNEGAN, L.L.P George Vande Sande Pollock, Vande Sande & Priddy, R.L. P.O. Box 19088 Washington, D.C. 20036-3425 U.S. that all statements made on information and be ements and the like so made are punishable by the validity of the application or any patent is	i the national or PCT, abandoned) abandoned) ark Office connected of the policy of t
(U.S. Application Seria (U.S. Application Ser	etined in 37 CFR § 1 ation: I No.) eys and/or agents to p 30.382; Aziz M. Ahs VI K. Neff, Reg. No. 28.9; No. 17,276, Rober 3,741, Townsend M. 1 ouis Woo, Reg. No. 3 OCK, VANDE SANE eph C. Redmond, Jr., ondence and Direct T George Vande Sanc (202) 331-7111 is made herein of my are made with the kn I that such willful fals Roy Childs	(U.S. Filing Date) (U.S. Filing Date) (U.S. Filing Date) (U.S. Filing Date) prosecute this application and san, Reg. No. 32.100: Ira D. F. 38.253: Eric W. Petraske, Reg. 289; all of INTERNATIONAL t. R. Priddy. Reg. No. 20,169, Belser, Jr., Reg. No. 22,956; 1,730. Elzbieta Chlopecka, R. D. & PRIDDY: John E. Hoel, Reg. No. 18,753; all of MOI elephone Calls to: the cown knowledge are true and the cowner of the control of	(Status—patented, pending (Status—patented, pending transact all business in the Patent and Tradem Blecker, Reg. No. 29.894: Steven Capella, Reg. No. 28,459. H. Daniel Schnurmann, Reg. N. BUSINESS MACHINES CORPORATION: I Burton A. Amemick, Reg. No. 24.852. Stanle Morris Liss, Reg. No. 24.510. Martin Abrams leg. No. 32,767, Eric J. Franklin, Reg. No. 37. Reg. No. 26,279, Christopher A. Hughes, Reg. RGAN & FINNEGAN, L.L.P George Vande Sande Pollock, Vande Sande & Priddy, R.L. P.O. Box 19088 Washington, D.C. 20036—3425 U.S. that all statements made on information and be ements and the like so made are punishable by the validity of the application or any patent is ased) by Anne Flaker Date Vermont 05452	abandoned) abandoned) ark Office connected of the conne
(U.S. Application Seria I hereby appoint the following attornetherewith: Joseph P. Abate, Reg. No. D. Mortinger, Reg. No. 39,306; Dary Soucar, Reg. No. 32,440, Marc D. Sch No. 16,906, George Vande Sande, Re 24,351, Richard Wiener, Reg. No. 18 George R. Pettit, Reg. No. 27,369, Lo Wales, Reg. No. 39,413; all of POLLO A. Pennington, Reg. No. 32,588; Joseph Corresponding to the control of the con	etined in 37 CFR § 1 ation: al No.) eys and/or agents to p 30.382; Aziz M. Ahs I K. Neff, Reg. No. 28.9; No. 17.276, Rober 3,741, Townsend M. 1000; Woo, Reg. No. 30 OCK, VANDE SAND eph C. Redmond, Jr., ondence and Direct T George Vande Sand (202) 331-7111; as made herein of my are made with the kn I that such willful fals Roy Childs Road, Ess	(U.S. Filing Date) (I.S. Assistance of the possession of	(Status—patented, pending (Status—patented, pending transact all business in the Patent and Tradem Blecker, Reg. No. 29.894: Steven Capella, Reg. No. 28,459. H. Daniel Schnurmann, Reg. N. BUSINESS MACHINES CORPORATION: I Burton A. Amemick, Reg. No. 24.852. Stanle Morris Liss, Reg. No. 24.510. Martin Abrams leg. No. 32,767, Eric J. Franklin, Reg. No. 37. Reg. No. 26,279, Christopher A. Hughes, Reg. RGAN & FINNEGAN, L.L.P George Vande Sande Pollock, Vande Sande & Priddy, R.L. P.O. Box 19088 Washington, D.C. 20036—3425 U.S. that all statements made on information and be ements and the like so made are punishable by the validity of the application or any patent is ased) by Anne Flaker Date Vermont 05452	abandoned) , abandoned , No. 35,791, Steven , Selicit I. Pollock, Reg. No. 25,787 , 134 and Robert Sco. , No. 26,914, Edward L.P. , S.A. elief are believed to be fine or imprisonmen

Page Two

Full name of second joint inventor (if any): Louis L. Hsu	
	Date
Residence Address 7 Crosby Court, Fishkill, New York 12524	
Chizenship United States	
Post Office Address Same as Above	
Full name of third joint inventor (if any): Jence B. Kuang	
Inventor's Signature	Date
Residence Address 15 Four Winds Drive, Poughkeepsie, New York	12603
Citizenship Taiwan R.O.C.	
Post Office Address Same as Above	
Full name of fourth joint inventor (if any):	
Inventor's Signature	
Residence Address	
Citizenship	
Post Office Address	
Full name of fifth joint inventor (if any):	
Inventor's Signature	
Residence Address	
Citizensnip	
Post Office Address	
Full name of such paint inventor (if any):	
Full name of sixth joint inventor (if any):	Date
Residence Address	
Citizenship	
Post Office Address	
Full name of seventh joint inventor (if any):	
Inventor's Signature	Date
Residence Address	
Citizenship	
Post Office Address	
Full name of eighth joint inventor (if any):	
Inventor's Signature	Date
Residence Address	
Citizenship	
Post Office Address	

[X] See next page for additional inventors

DECLARATION FOR PATENT APPLICATION As a below-named inventor. I hereby declare that: My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES the specification of which: (check one) [XX] is attached hereto. [] was filed on ______ 19__, as United States Patent Application Serial No. or PCT International Application Number I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 CFR § 1.56(a). Prior Foreign Application(s): I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate listed below, or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed: Priority Claimed [][] (Application No.) (Country) (Day/Month/Year Filed) Yes No [][](Application No.) (Country) (Day/Month/Year Filed) Yes No [][](Application No.) (Country) (Day/Month/Year Filed) Yes No I hereby claim the benefit under Title 35. United States Code § 119(e) of any United States provisional application(s) listed below-Application No. 60/044 251 April 23, 1997 I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by 35 U.S.C. § 112. first paragraph, I acknowledge the duty to disclose material information as defined in 37 CFR § 1.56(a) which occurred between the filling date of the prior application and the national or PCT international filing date of this application: (U.S. Application Serial No.) (U.S. Filing Date) (Status-patented, pending, abandoned) (U.S. Application Serial No.) (U.S. Filing Date) (Status-patented, pending, abandoned) I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Joseph P. Abate, Reg. No. 30,382; Aziz M. Ahsan, Reg. No. 32,100; Ira D. Blecker, Reg. No. 29,894; Steven Capella, Reg. No. 33,086; Alison D. Mortinger, Reg. No. 39,306, Daryl K. Neff, Reg. No. 38,253; Eric W. Petraske, Reg. No. 28,459, H. Daniel Schnurmann, Reg. No. 35,791, Steven J. Soucar, Reg. No. 32,440, Marc D. Schechter, Reg. No. 28,989; all of INTERNATIONAL BUSINESS MACHINES CORPORATION; Elliott I. Pollock, Reg. No. 16,906, George Vande Sande, Reg. No. 17,276, Robert R. Priddy, Reg. No. 20,169, Burton A. Amernick, Reg. No. 24,852, Stanley B. Green, Reg. No. 24,351, Richard Wiener, Reg. No. 18,741, Townsend M. Belser, Jr., Reg. No. 22,956; Morris Liss, Reg. No. 24,510, Martin Abramson, Reg. No. 25,787, George R. Pettil Reg. No. 27,369. Louis Woo, Reg. No. 31,730, Elzbieta Chlopecka, Reg. No. 32,767. Eric J. Franklin, Reg. No. 37,134 and Robert Scott Wales, Reg. No. 39,413; all of POLLOCK, VANDE SANDE & PRIDDY: John E. Hoel, Reg. No. 26,279, Christopher A. Hughes, Reg. No. 26,914, Edward A. Pennington, Reg. No. 32,588; Joseph C. Redmond, Jr., Reg. No. 18,753; all of MORGAN & FINNEGAN, L.L.P. Send Correspondence and Direct Telephone Calls to: George Vande Sande George Vande Sande Pollock, Vande Sande & Priddy, R.L.L.P. (202) 331-7111 P.O. Box 19088 Washington, D.C. 20036-3425 U.S.A. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment. or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. Full name of sole or first inventor: Roy Childs Flaker (deceased) by Heather Flaker (heir) Inventor's Signature X 750 Residence Address 2 Ridge Road, Essex Junction, Vermont 05452 Citizenship United States Post Office Address Same as Above

Page Two

Full name of second joint inventor (if any): Louis L. Hsu	
Inventor's Signature	
Residence Address 7 Crosby Court, Fishkill, New York 12524	
Citizenship United States	
Post Office Address Same as Above	
Full name of third joint inventor (if any): Jente B. Kuang	
Inventor's Signature	Date
Residence Address 15 Four Winds Drive, Poughkeepsie, New York	12603
Citizenship Taiwan R.O.C.	
Post Office Address Same as Above	
Full name of fourth joint inventor (if any):	
Inventor's Signature	
Residence Address	
Citizenship	
Post Office Address	
Full name of fifth joint inventor (if any):	
Inventor's Signature	
Residence Address	
Citizenship	
Post Office Address	
Full name of sixth joint inventor (if any):	
Inventor's Signature	
Residence Address	
Citizenship	
Post Office Address	
Full name of seventh joint inventor (if any):	
Inventor's Signature	Date
Residence Address	
Citizenship	
Post Office Address	
Full name of eighth joint inventor (if any):	
Inventor's Signature	Date
Residence Address	
Citizenship	
Post Office Address	

.::=4
100
u
Œ
Щ
, ,
- 1
- 1
::

Citizenship **United States**

Post Office Address <u>Same as Above</u>
[X] See next page for additional inventors

DECLARATION FOR PATENT APPLICATION As a below-named inventor, I hereby declare that: My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES the specification of which: (check one) [XX] is attached hereto. was filed on 19, as United States Patent Application Serial No. or PCT International Application Number I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 CFR § 1.56(a). Prior Foreign Application(s): I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate listed below, or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed: Priority Claimed [][](Application No.) (Country) (Day/Month/Year Filed) Yes No [][] (Application No.) (Country) (Day/Month/Year Filed) Yes No. [][] (Application No.) (Country) (Day/Month/Year Filed) Yes No I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below Application No. Filing Date 60/044,251 April 23, 1997 I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by 35 U.S.C § 112, first paragraph. I acknowledge the duty to disclose material information as defined in 37 CFR § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application: (U.S. Application Serial No.) (U.S. Filing Date) (Status-patented, pending, abandoned) (U.S. Application Serial No.) (U.S. Filing Date) (Status--patented, pending, abandoned) I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Joseph P. Abate, Reg. No. 30.382; Aziz M. Ahsan, Reg. No. 32,100; Ira D. Blecker, Reg. No. 29,894; Steven Capella, Reg. No. 33,086, Alison D. Mortinger, Reg. No. 39,306; Daryl K. Neff, Reg. No. 38,253; Eric W Petraske, Reg. No. 28,459. H. Daniel Schnurmann, Reg. No. 35,791, Steven J. Soucar, Reg. No. 32,440, Marc D. Schechter, Reg. No. 28.989; all of INTERNATIONAL BUSINESS MACHINES CORPORATION; Elliott I. Pollock, Reg. No. 16,906, George Vande Sande, Reg. No. 17,276, Robert R. Priddy, Reg. No. 20,169, Burton A. Amernick, Reg. No. 24,852, Stanley B. Green, Reg. No. 24.351, Richard Wiener, Reg. No. 18.741, Townsend M. Belser, Jr., Reg. No. 22.956; Morris Liss, Reg. No. 24,510, Martin Abramson, Reg. No. 25.787, George R. Pettit, Reg. No. 27.369. Louis Woo, Reg. No. 31.730. Elzbieta Chlopecka, Reg. No. 32.767, Eric J. Franklin, Reg. No. 37.134 and Robert Scott Wales, Reg. No. 39.413; all of POLLOCK, VANDE SANDE & PRIDDY; John E. Hoel, Reg. No. 26.279. Christopher A. Hughes, Reg. No. 26.914, Edward A. Pennington, Reg. No. 32.588; Joseph C. Redmond, Jr., Reg. No. 18,753; all of MORGAN & FINNEGAN, L.L.P. Send Correspondence and Direct Telephone Calls to: George Vande Sande George Vande Sande Pollock, Vande Sande & Priddy, R.L.L.P. (202) 331-7111 P.O. Box 19088 Washington, D.C. 20036-3425 U.S.A. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment. or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. Full name of sole or first inventor: Roy Childs Flaker (deceased) Date Residence Address 2 Ridge Road, Essex Junction, Vermont 05452

Page Two

Inventor's Signature	Date _	3/26/98
Residence Address 7 Crosby Court, Fishkill, New York 12524		
Citizenship <u>United States</u>		
Post Office Address Same as Above		
Full name of third joint inventor (if any): Jente B. Kuang		
Inventor's Signature		4/8/1998
Residence Address 15 Four Winds Drive, Poughkeepsie, New York	1260	03
Citizenship Taiwan R.O.C.		
Post Office Address Same as Above		
Full name of fourth joint inventor (if any):		
Inventor's Signature	Date	
Residence Address		
Citizenship		
Post Office Address		
Full name of fifth joint inventor (if any):		
Inventor's Signature	Date	
Residence Address		
Citizenship		
Post Office Address		
Full name of sixth joint inventor (if any):		
inventor's Signature	Date	
inventor's Signature	Date	
Residence Address	Date	
inventor's Signature	Date	
Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any):	Date	
Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature	Date	
Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature	Date	
Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Residence Address	Date	
Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Residence Address	Date	
Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Full name of eighth joint inventor (if any):	Date	
Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Citizenship Full name of eighth joint inventor (if any): Inventor's Signature	Date	
Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Citizenship Full name of eighth joint inventor (if any): Inventor's Signature	Date	
Residence Address Citizenship Post Office Address Full name of seventh joint inventor (if any): Inventor's Signature Residence Address Citizenship Post Office Address Full name of eighth joint inventor (if any):	Date	